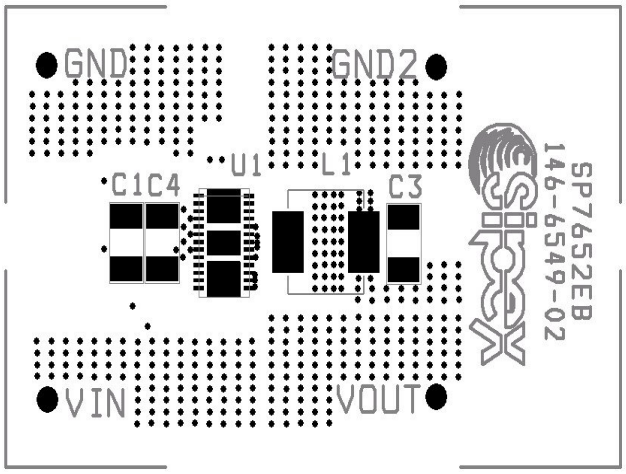
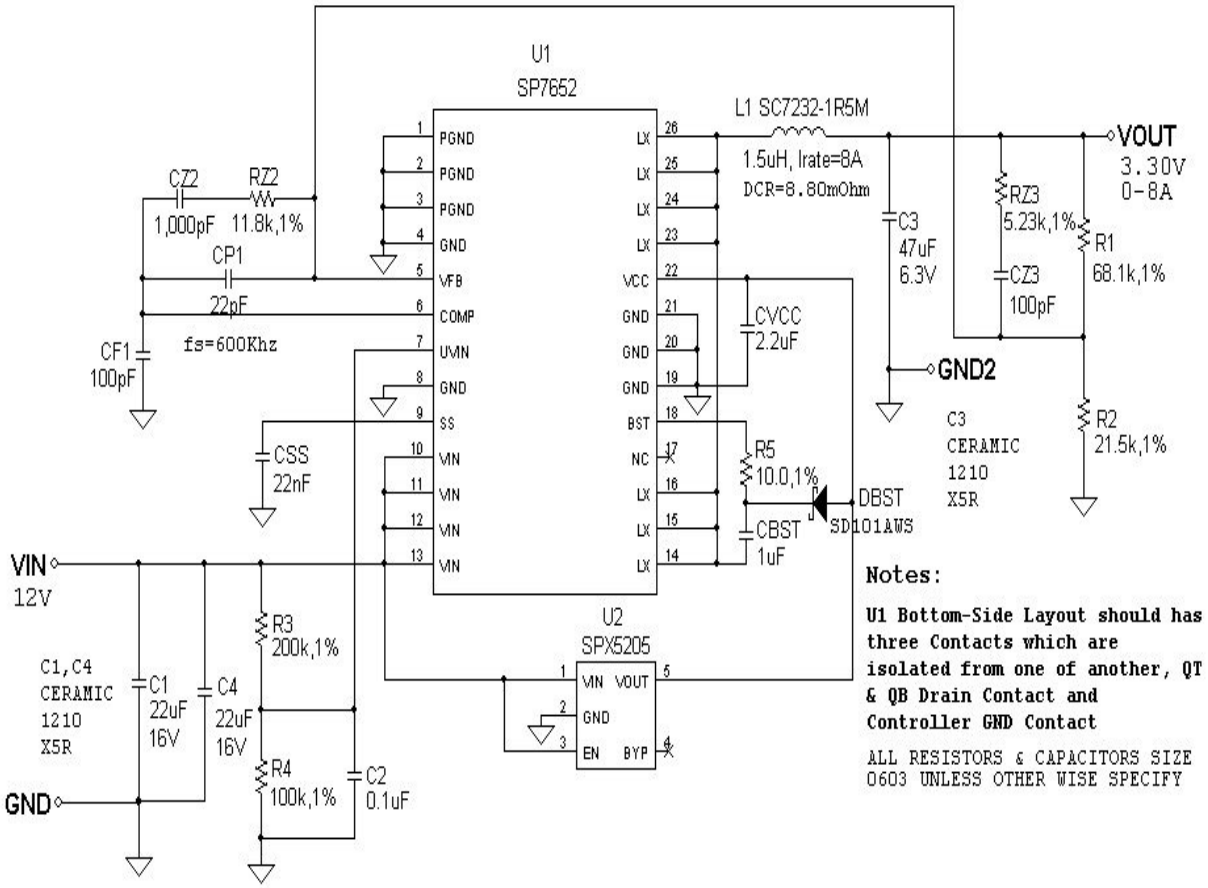
SP7652

Evaluation Board Manual

- Easy Evaluation of the SP7652ER 600kHz, 6A PowerBlox™ Device
- Built in Low Rds(on) Power FETs
- UVLO Detects Both VCC and VIN
- High Integrated Design, Minimal Components
- High Efficiency: 90%
- Feature Rich: UVIN, Programmable Softstart, External VCC Supply and Output Dead Short Circuit Shutdown Protection



SP7652EB SCHEMATIC



USING THE EVALUATION BOARD

1) Powering Up the SP7652EB Circuit

Connect the SP7652 Evaluation Board with an external +12V power supply. Connect with short leads and large diameter wire directly to the “VIN” and “GND” posts. Connect a Load between the VOUT and GND2 posts, again using short leads with large diameter wire to minimize inductance and voltage drops.

2) Measuring Output Load Characteristics

It’s best to GND reference scope and digital meters using the Star GND post in the center of the board. VOUT ripple can best be seen touching probe tip to the pad for C3 and scope GND collar touching Star GND post – avoid a GND lead on the scope which will increase noise pickup.

3) Using the Evaluation Board with Different Output Voltages

While the SP7652 Evaluation Board has been tested and delivered with the output set to 3.30V, by simply changing one resistor, R2, the SP7652 can be set to other output voltages. The relationship in the following formula is based on a voltage divider from the output to the feedback pin VFB, which is set to an internal reference voltage of 0.80V.
Standard 1% metal film resistors of surface mount size 0603 are recommended.

$$Vout = 0.80V \left(R1 / R2 + 1 \right) \Rightarrow R2 = R1 / \left[\left(Vout / 0.80V \right) - 1 \right]$$

Where R1 = 68.1KΩ and for Vout = 0.80V setting, simply remove R2 from the board. Furthermore, one could select the value of R1 and R2 combination to meet the exact output voltage setting by restricting R1 resistance range such that $50K\Omega \leq R1 \leq 100K\Omega$ for overall system loop stability.

Note that since the SP7652 Evaluation Board design was optimized for 12V down conversion to 3.30V, changes of output voltage and/or input voltage will alter performance from the data given in the Power Supply Data section. In addition, the SP7652EU provides short circuit protection by sensing Vout at GND.

POWER SUPPLY DATA

The SP7652EU is designed with a very accurate 1.0% reference over line, load and temperature. Figure 1 data shows a typical SP7652 Evaluation Board Efficiency plot, with efficiencies to 90% and output currents to 8A. SP7652EU Load Regulation is shown in Figure 2 of only 0.4% change in output voltage from no load to 8A load. Figures 3 and 4 illustrate a 4A to 8A and 0A to 8A Load Step. Start-up Response in Figures 5, 6 and 7 show a controlled start-up with different output load behavior when power is applied where the input current rises smoothly as the Softstart ramp increases. In Figure 8 the SP7652EU is configured for hiccup mode in response to an output dead short circuit condition and will Softstart until the over-load is removed. Figure 9 and 10 show output voltage ripple less than 50mV at no load to 8A load.

While data on individual power supply boards may vary, the capability of the SP7652EU of achieving high accuracy over a range of load conditions shown here is quite impressive and desirable for accurate power supply design.

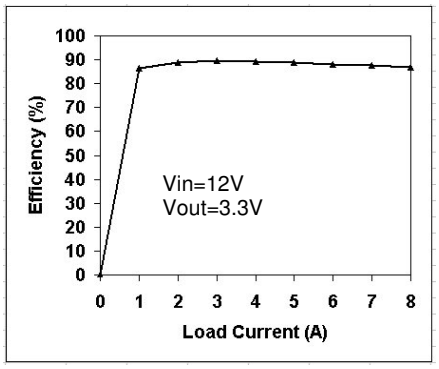


Figure 1. Efficiency vs Load

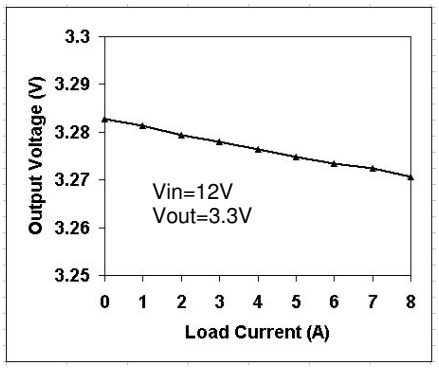


Figure 2. Load Regulation

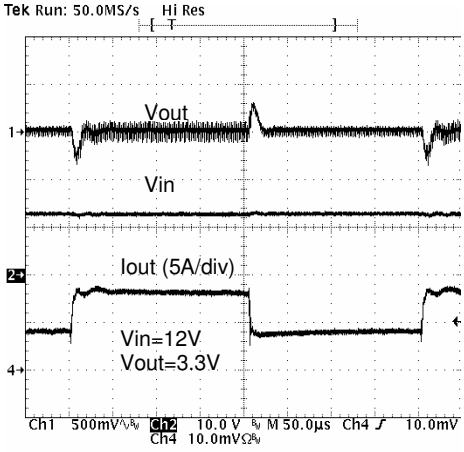


Figure 3. Load Step Response: 4->8A

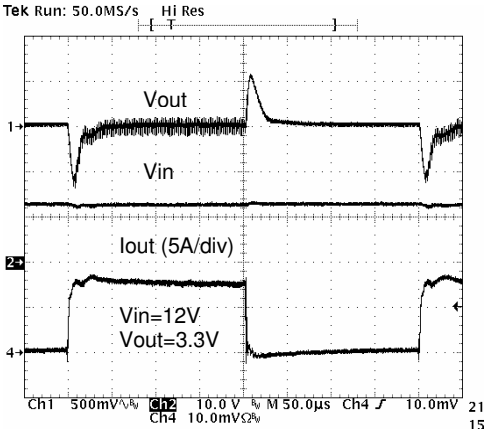


Figure 4. Load Step Response: 0->8A

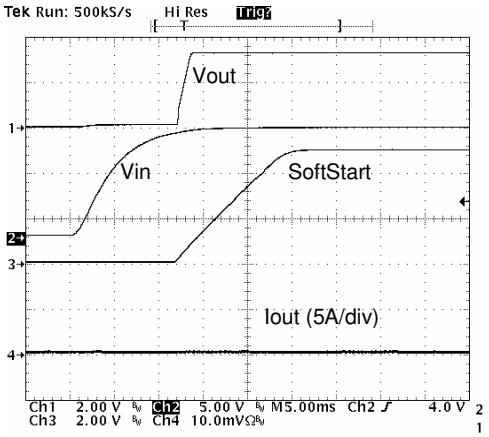


Figure 5. Start-Up Response: No Load

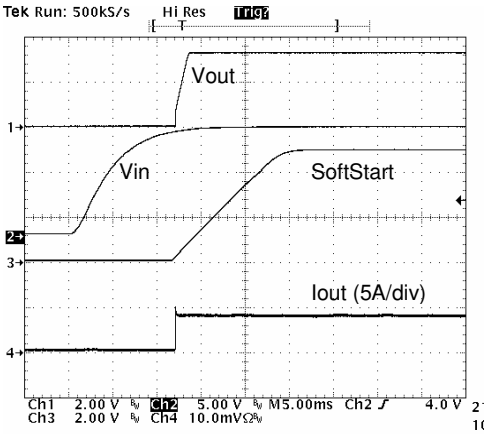


Figure 6. Start-Up Response: 4A Load

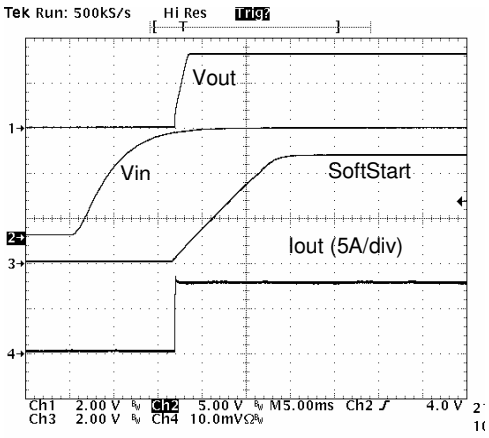


Figure 7. Start-Up Response: 8A Load

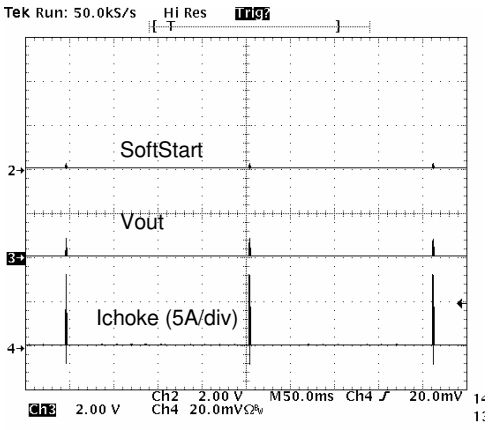
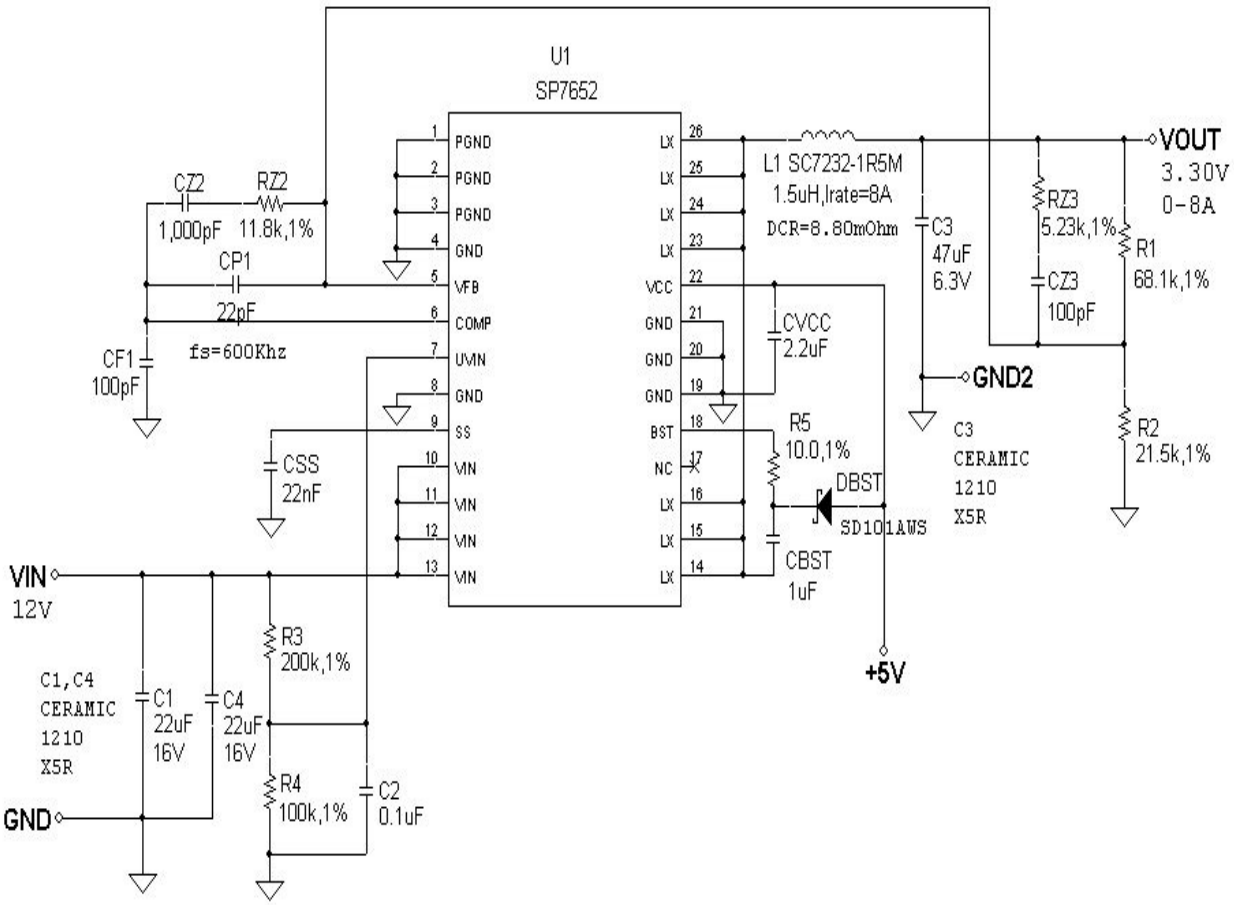


Figure 8. Output Load Short Circuit

+5V BIAS SUPPLY APPLICATION SCHEMATIC

In this application example, the SP7652EU is power by an external +5V bias supply which current consumption of 20mA Maximum. If this supply is not available than it is recommend Sipex SPX5205 Low-Noise LDO Voltage Regulator which is included on the SP7652 Evaluation Board.



DIFFERENT +5V BIAS SUPPLY SCHEMES APPLICATION SCHEMATIC

The SP7652EU VCC Bias Supply can be derived from Vin or external bias with several biasing options. The transistor plus zener diode +5V bias supply could also be used as shown in Figure 11.

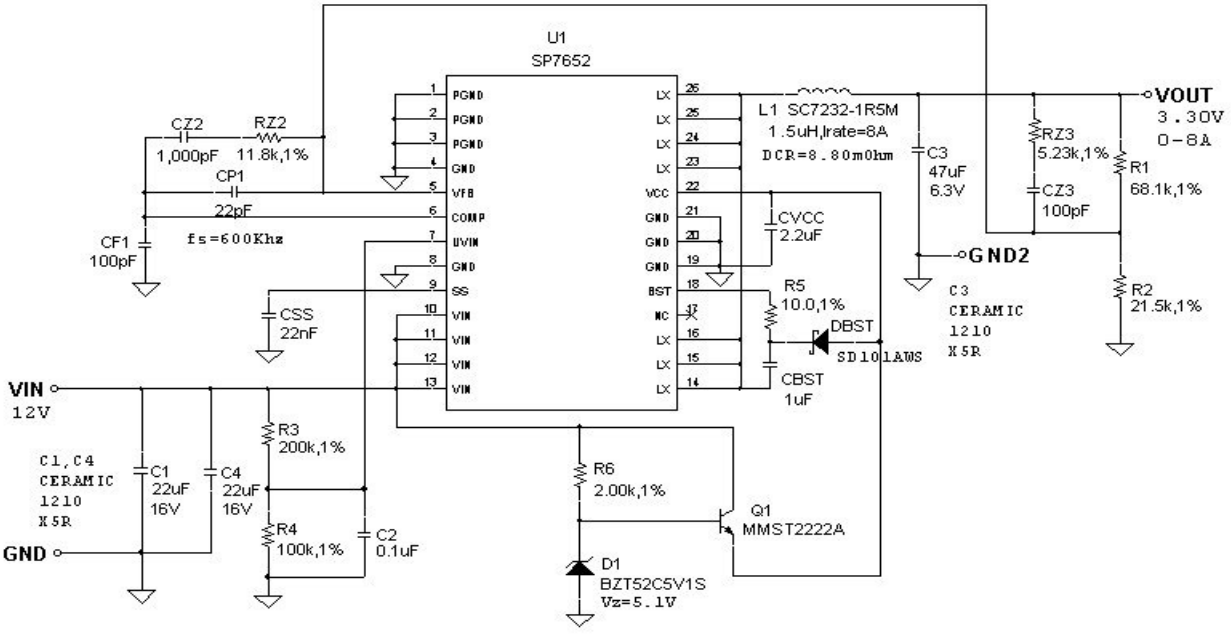


Figure 11. Transistor plus Zener Diode +5V Supply Application Schematic

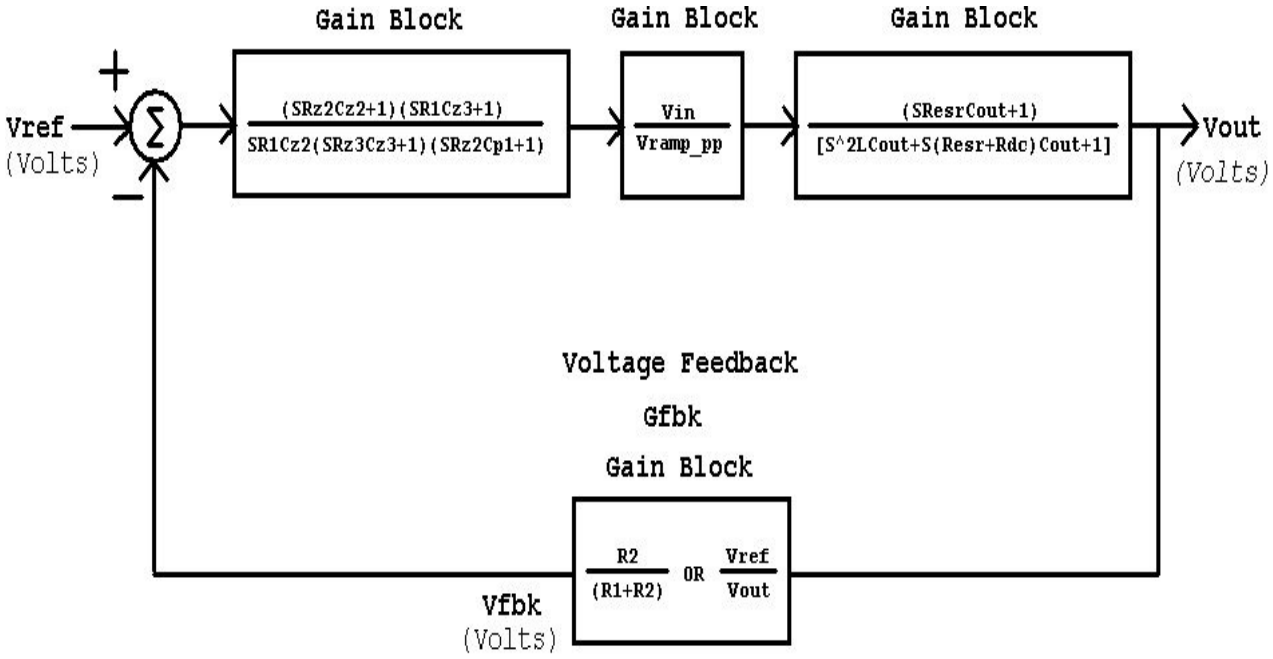
Table 1: SP7652EB Suggested Components and Vendor Lists

INDUCTORS - SURFACE MOUNT							
Inductance (uH)	Manufacturer/Part No.	Inductor Specification					
		Series R mOhms	Isat (A)	Size LxW(mm)	Ht.(mm)	Inductor Type	Manufacturer Website
1.5	**Inter-Technical SC7232-1R5M**	**8.8**	**13**	**6.8x6.8**	**4.5**	**Shielded Ferrite Core**	www.inter-technical.com
1.5	Coilcraft DO3316P-152	9.0	8.0	12.95x9.40	5.5	Non-Shielded Ferrite Core	www.coilcraft.com
CAPACITORS - SURFACE MOUNT							
Capacitance(uF)	Manufacturer/Part No.	Capacitor Specification					
		ESR mOhms (max)	Ripple Current (A) @ 45C	Size LxW(mm)	Ht.(mm)	Voltage (V)	Capacitor Type / Manufacturer Website
22	**TDK C3225X5R1C226M**	**2.0**	**4.0**	**3.2x2.5**	**2.0**	**16.0**	**X5R Ceramic** / www.tdk.com
47	**TDK C3225X5R0J476M**	**2.0**	**4.0**	**3.2x2.5**	**2.5**	**6.3**	**X5R Ceramic** / www.tdk.com

Note: Components highlighted in **bold** are those used on the SP7652 Evaluation Board.

LOOP COMPENSATION DESIGN

The open loop gain of the SP7652EB can be divided into the gain of the error amplifier **Gamp(s)**, PWM modulator **Gpwm**, buck converter output stage **Gout(s)**, and feedback resistor divider **Gfbk**. In order to crossover at the selecting frequency **fco**, the
gain of the error amplifier has to compensate for the attenuation caused by the rest of the loop at this frequency. The goal of loop compensation is to manipulate the open loop frequency response such that its gain crosses over 0dB at a slope of –20dB/dec.
The open loop crossover frequency should be higher than the ESR zero of the output capacitors but less than 1/5 to 1/10 of the switching frequency **fs** to insure proper operation. Since the SP7652EB is designed with Ceramic Type output capacitors, a Type III compensation circuit is required to give a phase boost of 180° in order to counteract the effects of the output **LC** under damped resonance double pole frequency.



Definitions:

Resr := Output Capacitor Equivalent Series Resitance

Rdc := Output Inductor DC Resistance

Vramp_pp := SP7652 Internal RAMP Amplitude Peak to Peak Voltage

Conditions:

Cz2 >> Cp1 and R1 >> Rz3

Output Load Resistance >> Resr and Rdc

Note: Loop Compensation component calculations discussed in this section are further elaborated in the application note #ANP16, "**Loop Compensation of Voltage-Mode Buck Converters".** These calculations shown here can be quickly iterated with the Type III Loop Compensation Calculator on the web at:
www.sipex.com/files/Application-Notes/TypeIIICalculator.xls

Figure 12. SP7652EB Voltage Mode Control Loop with Loop Dynamic

The simple guidelines for positioning the poles and zeros and for calculating the component values for Type III compensation are as follows.

a. Choose **fco** = fs / 10

b. Calculate **fp_LC**
fp_LC = 1 / 2π [(L) (C)] ^ 1/2

c. Calculate **fz_ESR**
fz_ESR = 1 / 2π (Resr) (Cout)

d. Select **R1** component value such that 50kΩ ≤ R1 ≤ 100kΩ

e. Calculate **R2** base on the desired Vout
R2 = R1 / [(Vout / 0.80V) – 1]

f. Select the ratio of **Rz2** / **R1** gain for the desired gain bandwidth
Rz2 = R1 (Vramp_pp / Vin_max) (fco / fp_LC)

g. Calculate **Cz2** by placing the zero at ½ of the output filter pole frequency
Cz2 = 1 / π (Rz2) (fp_LC)

h. Calculate **Cp1** by placing the first pole at ESR zero frequency
Cp1 = 1 / 2π (Rz2) (fz_ESR)

i. Calculate **Rz3** by setting the second pole at ½ of the switching frequency and the second zero at the output filter double pole frequency
Rz3 = 2 (R1) (fp_LC) / fs

j. Calculate **Cz3** from **Rz3** component value above
Cz3 = 1 / π (Rz3) (fs)

k. Choose 100pF ≤ **Cf1** ≤ 220pF to stabilize the SP7652EU internal Error Amplify

As a particular example, consider for the following SP7652EB with a type III Voltage Loop Compensation component selections:

Vin = 5 to 15V
Vout = 3.30V @ 0 to 8A load
Select **L = 1.5uH** => yield ≈ 35% of maximum 8A output current ripple.
Select **Cout = 47uF** Ceramic capacitors (Resr ≈ 2mΩ)
fs = 600khz SP7652 internal Oscillator Frequency
Vramp_pp = 1.0V SP7652 internal Ramp Peak to Peak Amplitude

Step by step design procedures:

a. **fco** = 600khz / 10 = 60khz

b. **fp_LC** = 1 / 2π [(1.5uH)(47uF)]^1/2 ≈ 20khz

c. **fz_ESR** = 1 / 2π (2mΩ)(47uF) ≈ 1.7Mhz

d. **R1** = 68.1kΩ, 1%

e. **R2** = 68.1kΩ / [(3.30V / 0.80V) – 1] ≅ 21.5kΩ, 1%

f. **Rz2** = 68.1kΩ (1.0V / 15V) (60khz / 20khz) ≈ 11.8kΩ, 1%

g. **Cz2** = 1 / π (11.8kΩ) (20khz) ≈ 1,000pF, X7R

h. **Cp1** = 1 / 2π (11.8kΩ) (1.7Mhz) ≈ 10pF => Select **Cp1** = 22pF for noise filtering

i. **Rz3** = 2 (68.1kΩ) (20khz) / 600khz ≈ 5.23kΩ, 1%

j. **Cz3** = 1 / π (5.23kΩ) (600khz) ≅ 100pF, COG

k. **Cf1** = 100pF to stabilize SP7652EU internal Error Amplify

PC LAYOUT DRAWINGS

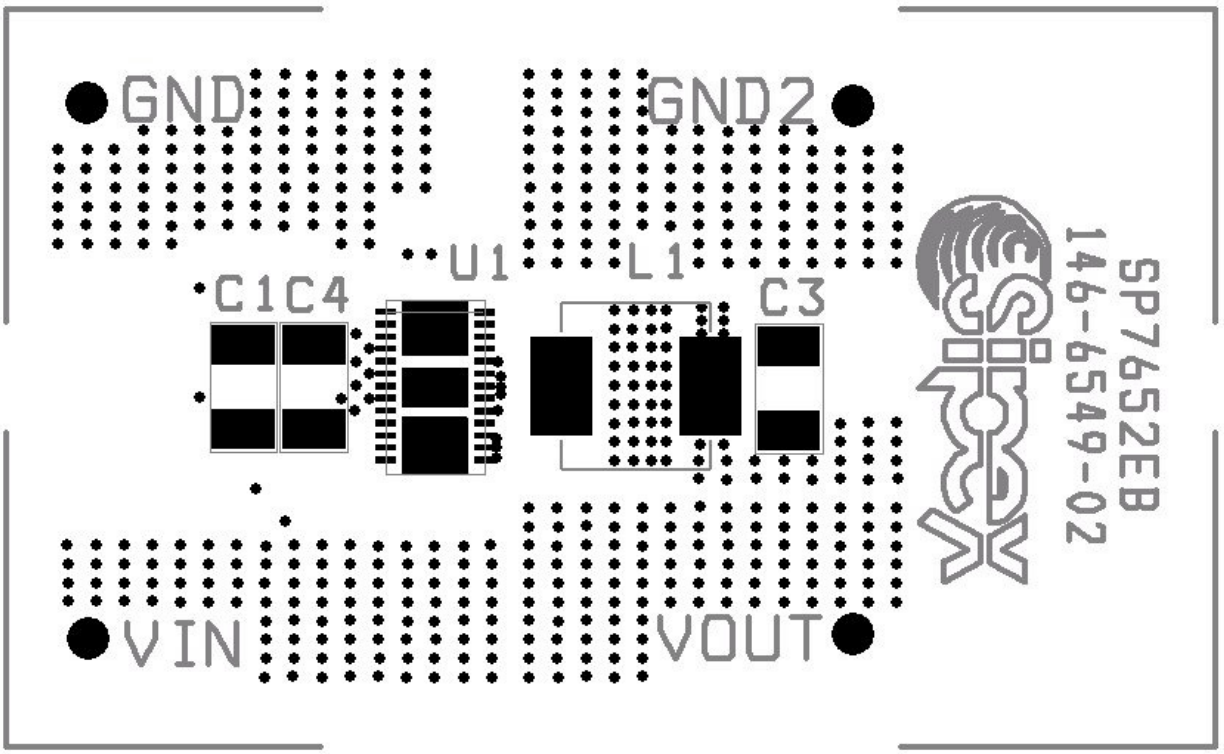


Figure 13. SP7652EB Component Placement

PC LAYOUT DRAWINGS

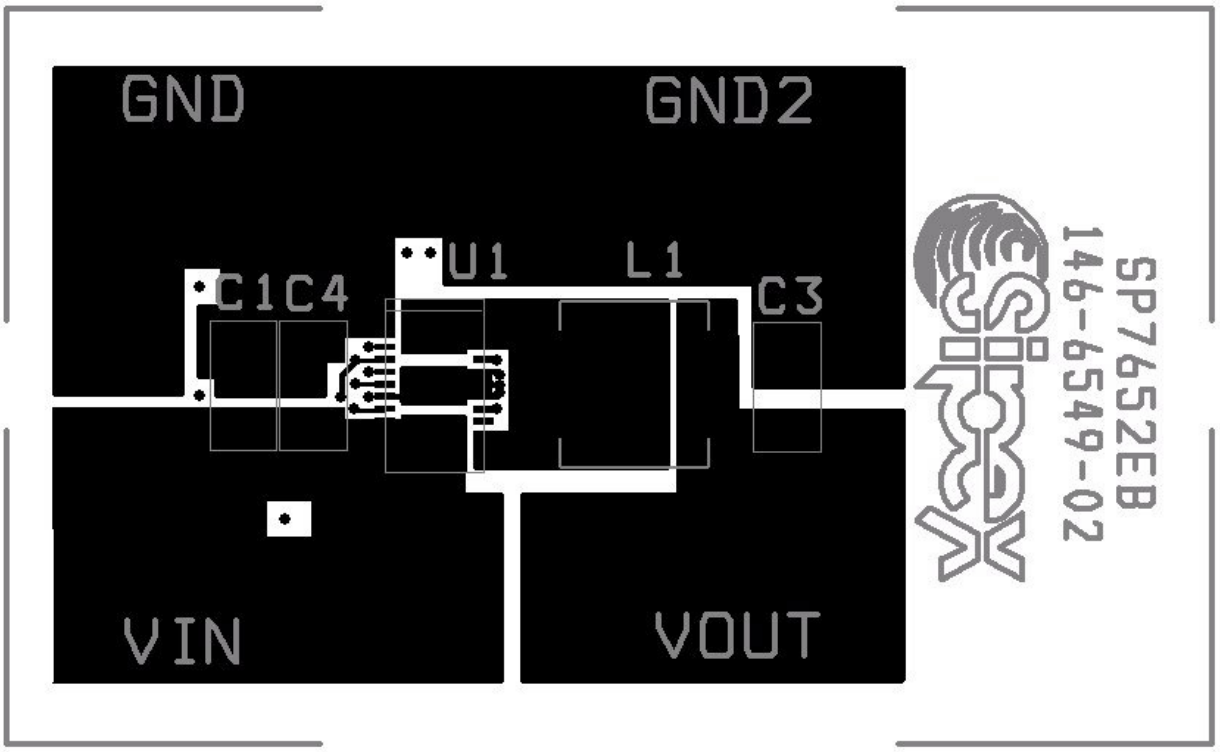


Figure 14. SP7652EB PC Layout Top Side

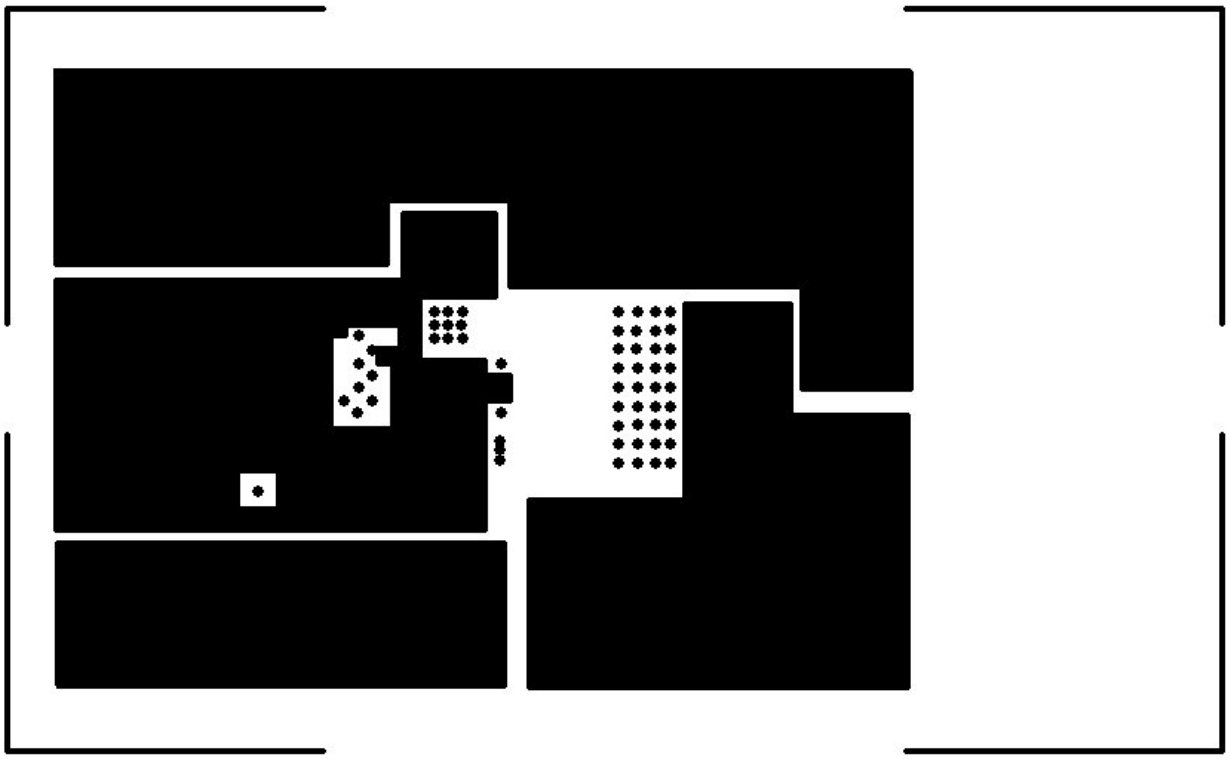


Figure 15. SP7652EB PC Layout 2nd Layer Side

PC LAYOUT DRAWINGS

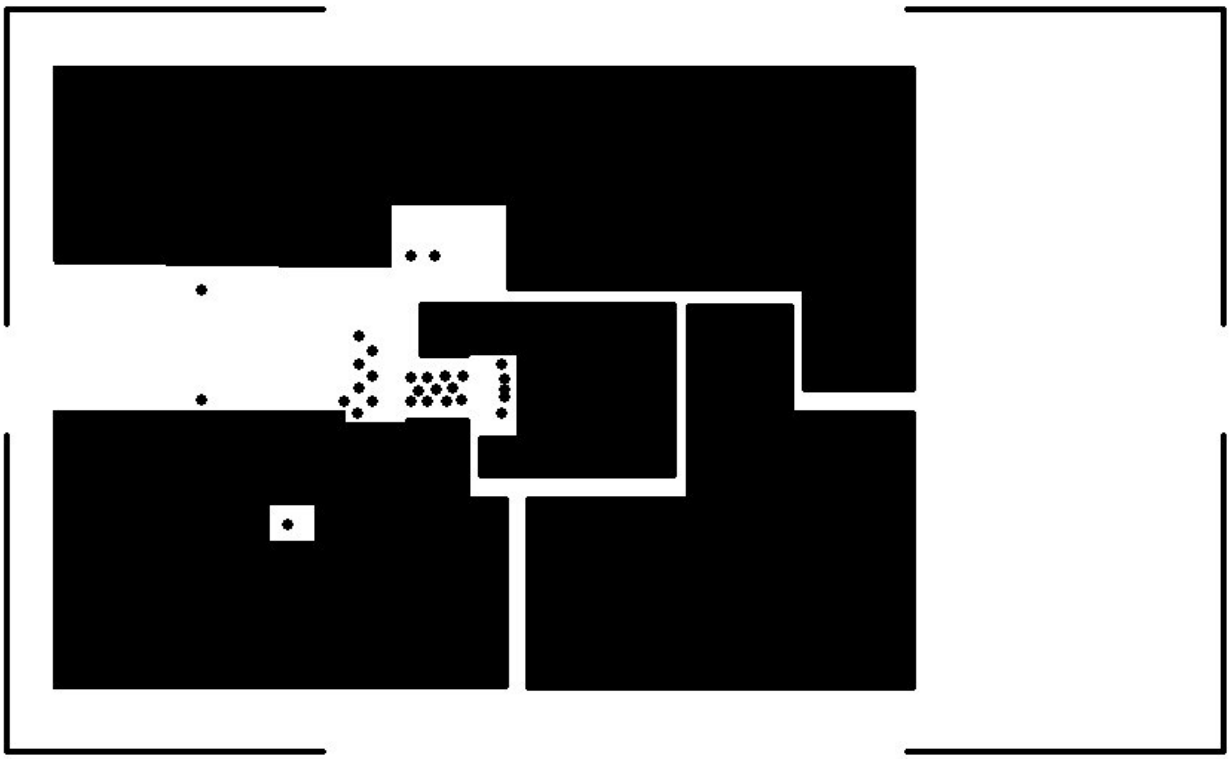


Figure 16. SP7652EB PC Layout 3rd Layer Side

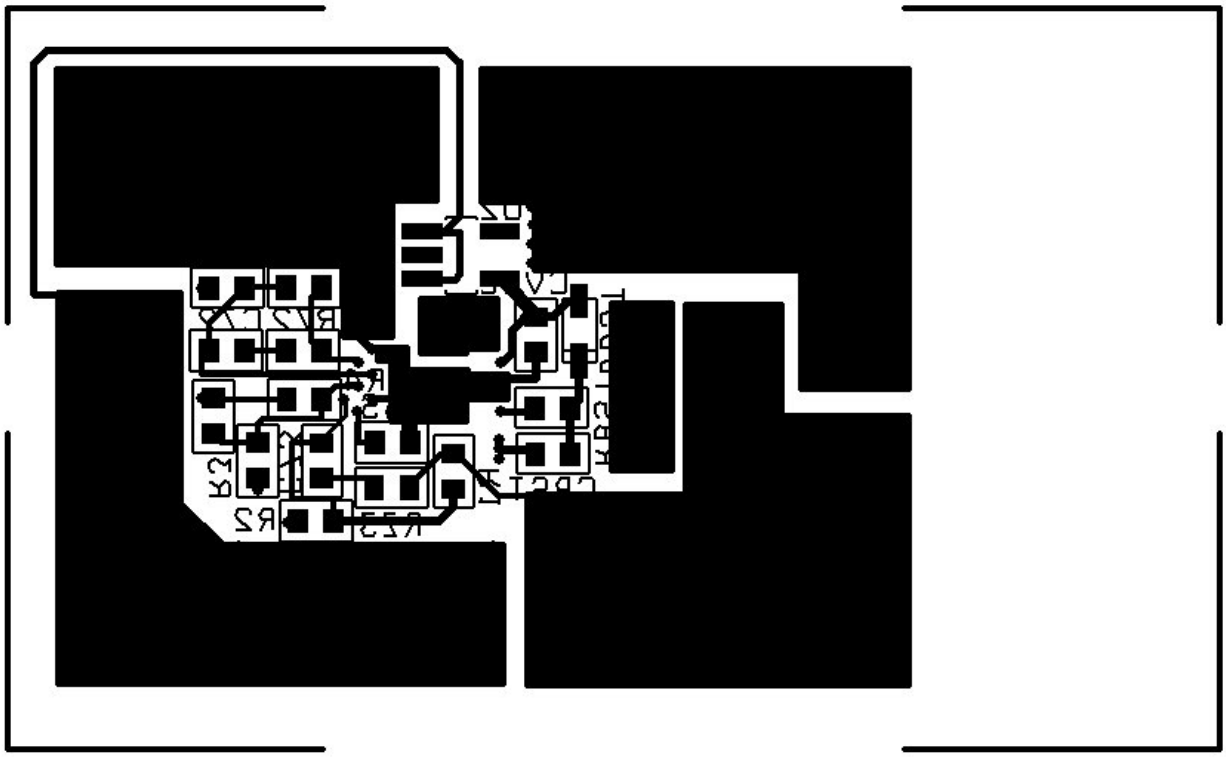


Figure 17. SP7652EB PC Layout Bottom Side

			SP7652 Evaluation Board Rev. 02 List of Materials				4/21/2004
Line No.	Ref. Des.	Qty.	Manuf.	Manuf. Part Number	Layout Size	Component	Vendor Phone Number
1	PCB	1	Sipex	146-6549-02	1.75"X2.75"	SP7652EB	978-667-7800
2	U1	1	Sipex	SP7652EU	DFN-26	2-FETs Buck Ctrl	978-667-7800
3	U2	1	Sipex	SPX5205M5-5.0	SOT-23-5	150mA LDO Voltage Reg	978-667-7800
4	DBST	1	Vishay Semi	SD101AWS	SOD-323	15mA Schottky Diode	800-344-4539
5	L1	1	Inter-Technical	SC7232-1R5M	6.8X6.8mm	1.5uH Coil 8A 8.80mohm	914-347-2474
6	C3	1	TDK	C3225X5R0J476M	1210	47uF Ceramic X5R 6.3V	978-779-3111
7	C1,C4	2	TDK	C3225X5R1C226M	1210	22uF Ceramic X5R 16V	978-779-3111
8	CVCC	1	TDK	C1608X5R1A225K	0603	2.2uF Ceramic X5R 10V	978-779-3111
9	CBST	1	TDK	C1608X5R1A105K	0603	1.0uF Ceramic X5R 10V	978-779-3111
10	C2	1	TDK	C1608X7R1H104K	0603	0.1uF Ceramic X7R 50V	978-779-3111
11	CSS	1	TDK	C1608X7R1H223K	0603	22,000pF Ceramic X7R 50V	978-779-3111
12	CP1	1	TDK	C1608COG1H220J	0603	22pF Ceramic COG 50V	978-779-3111
13	CZ2	1	TDK	C1608COG1H102J	0603	1,000pF Ceramic COG 50V	978-779-3111
14	CF1, CZ3	2	TDK	C1608COG1H101J	0603	100pF Ceramic COG 50V	978-779-3111
15	RZ2	1	Panasonic	ERJ-3EKF1182V	0603	11.8K Ohm Thick Film Res 1%	800-344-4539
16	R2	1	Panasonic	ERJ-3EKF2152V	0603	21.5K Ohm Thick Film Res 1%	800-344-4539
17	RZ3	1	Panasonic	ERJ-3EKF5231V	0603	5.23K Ohm Thick Film Res 1%	800-344-4539
18	R1	1	Panasonic	ERJ-3EKF6812V	0603	68.1K Ohm Thick Film Res 1%	800-344-4539
19	R3	1	Panasonic	ERJ-3EKF2003V	0603	200K Ohm Thick Film Res 1%	800-344-4539
20	RBST	1	Panasonic	ERJ-3EKF10R0V	0603	10.0 Ohm Thick Film Res 1%	800-344-4539
21	R4	1	Panasonic	ERJ-3EKF1003V	0603	100K Ohm Thick Film Res 1%	800-344-4539
22	VIN, VOUT, GND, GND2	4	Vector Electronic	K24C/M	.042 Dia	Input/Output Terminal Posts	800-344-4539

Table 2: SP7652EB List of Materials

ORDERING INFORMATION

Model	Temperature Range	Package Type
SP7652EB	-40°C to +85°C	SP7652 Evaluation Board
SP7652EU	-40°C to +85°C	26-pin DFN

For further assistance:

Email: Sipexsupport@sipex.com
WWW Support page: http://www.sipex.com/content.aspx?p=support
Sipex Application Notes: http://www.sipex.com/applicationNotes.aspx
Loop Compensation Calculator www.sipex.com/files/Application-Notes/TypeIIICalculator.xls

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