

74LVCH322244A

32-bit buffer/line driver; 30 Ω series termination resistors; 5 V tolerant input/output; 3-state

Rev. 3 — 16 December 2011

Product data sheet

1. General description

The 74LVCH322244A is a 32-bit non-inverting buffer/line driver with 3-state outputs. The 3-state outputs are controlled by the output enable inputs $\overline{\text{nOE}}$. A HIGH on input $\overline{\text{nOE}}$ causes the outputs to assume a high-impedance OFF-state.

The device is designed with 30 Ω series termination resistors in both HIGH and LOW output stages to reduce line noise.

To ensure the high-impedance state during power-up or power-down, input $\overline{\text{nOE}}$ should be tied to V_{CC} through a pull-up resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Inputs can be driven from either 3.3 V or 5 V devices. In 3-state operation, outputs can handle 5 V. These features allow the use of these devices in a mixed 3.3 V and 5 V environment.

Bus hold on data inputs eliminates the need for external pull-up resistors to hold unused or floating data inputs at a valid logic level.

2. Features and benefits

- 5 V tolerant inputs/outputs for interfacing with 5 V logic
- Wide supply voltage range from 1.2 V to 3.6 V
- CMOS low power consumption
- MULTIBYTE flow-through standard pin-out architecture
- Low inductance multiple power and ground pins for minimum noise and ground bounce
- Direct interface with TTL levels
- Integrated 30 Ω termination resistors
- All data inputs have bus hold
- Complies with JEDEC standard:
 - ◆ JESD8-7A (1.65 V to 1.95 V)
 - ◆ JESD8-5A (2.3 V to 2.7 V)
 - ◆ JESD8-C/JESD36 (2.7 V to 3.6 V)
- ESD protection:
 - ◆ HBM JESD22-A114F exceeds 2000 V
 - ◆ MM JESD22-A115-B exceeds 200 V
 - ◆ CDM JESD22-C101E exceeds 1000 V
- Specified from $-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$ and $-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$



- Packaged in plastic fine-pitch ball grid array package

3. Ordering information

Table 1: Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
74LVCH322244AEC	-40 °C to +85 °C	LFBGA96	plastic low profile fine pitch ball grid array package; 96 balls; body 13.5 × 5.5 × 1.05 mm	SOT536-1

4. Functional diagram

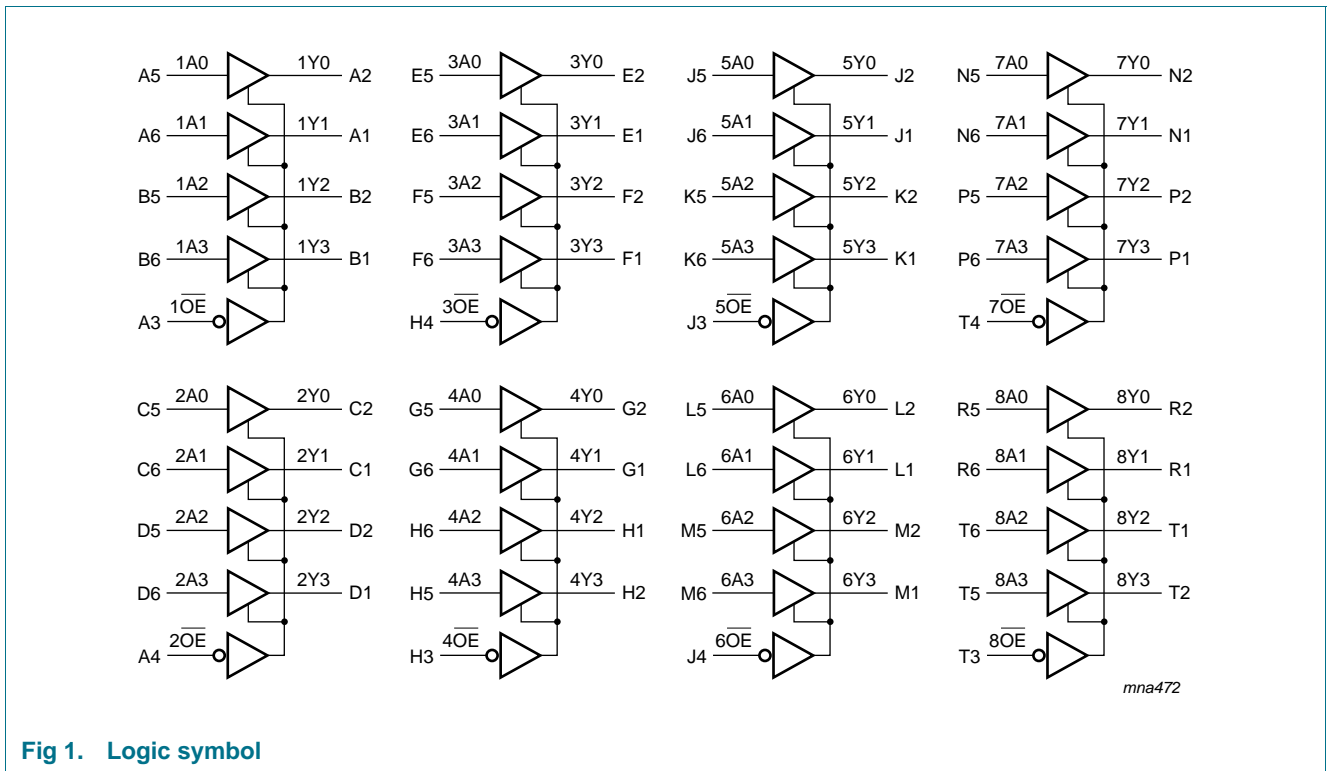


Fig 1. Logic symbol

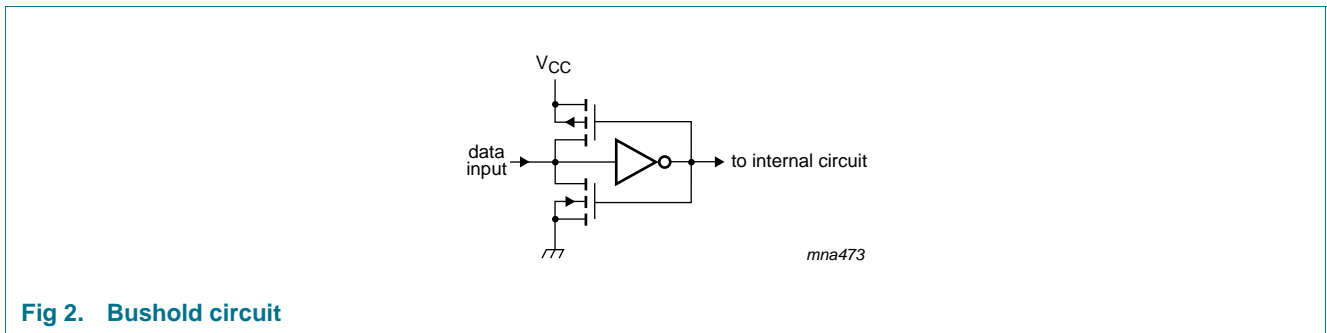
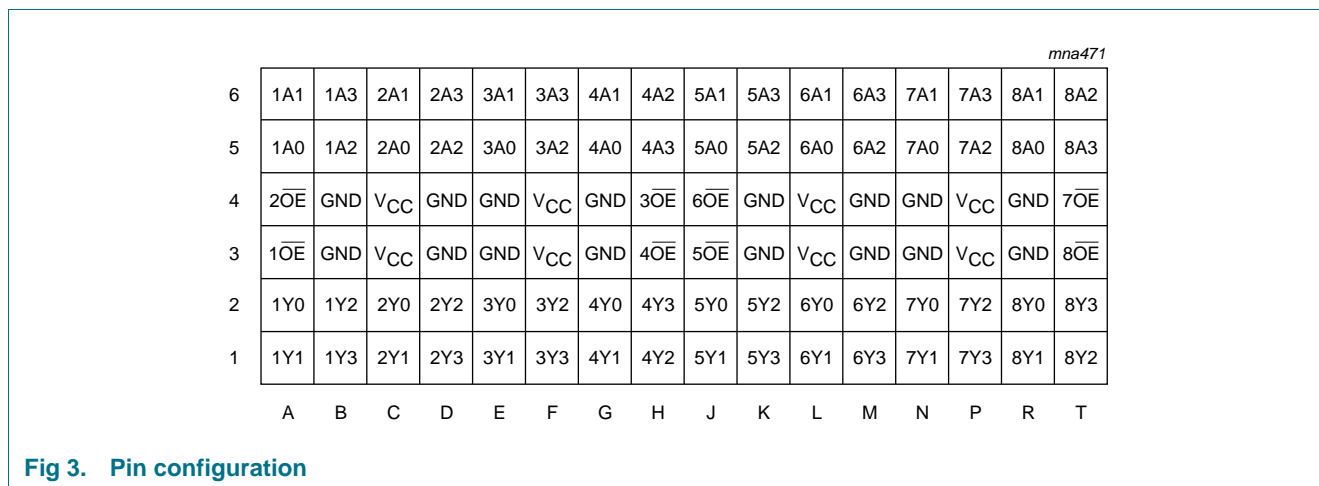


Fig 2. Bushold circuit

5. Pinning information

5.1 Pinning



5.2 Pin description

Table 2: Pin description

Ball	Symbol	Description
n \overline{OE} (n = 1 to 8)	A3, A4, H4, H3, J3 J4, T4, T3	3-state output enable inputs (active LOW)
1A[0:3]	A5, A6, B5, B6	data input
2A[0:3]	C5, C6, D5, D6	
3A[0:3]	E5, E6, F5, F6	
4A[0:3]	G5, G6, H6, H5	
5A[0:3]	J5, J6, K5, K6	
6A[0:3]	L5, L6, M5, M6	
7A[0:3]	N5, N6, P5, P6	
8A[0:3]	R5, R6, T6, T5	
1Y[0:3]	A2, A1, B2, B1	data output
2Y[0:3]	C2, C1, D2, D1	
3Y[0:3]	E2, E1, F2, F1	
4Y[0:3]	G2, G1, H1, H2	
5Y[0:3]	J2, J1, K2, K1	
6Y[0:3]	L2, L1, M2, M1	
7Y[0:3]	N2, N1, P2, P1	
8Y[0:3]	R2, R1, T1, T2	
V _{CC}	C3, C4, F3, F4, L3, L4, P3, P4	supply voltage
GND	B3, B4, D3, D4, E3, E4, G3, G4, K3, K4, M3, M4, N3, N4, R3, R4	ground (0 V)

6. Functional description

Table 3: Functional table^[1]

Input		Output
nOE	nAn	nYn
L	L	L
L	H	H
H	X	Z

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+6.5	V
I_{IK}	input clamping current	$V_I < 0$	-50	-	mA
V_I	input voltage		[1] -0.5	+6.5	V
I_{OK}	output clamping current	$V_O > V_{CC}$ or $V_O < 0$	-	± 50	mA
V_O	output voltage	output HIGH or LOW state	[2] -0.5	$V_{CC} + 0.5$	V
		output 3-state	[2] -0.5	+6.5	V
I_O	output current	$V_O = 0$ V to V_{CC}	-	± 50	mA
I_{CC}	supply current		-	200	mA
I_{GND}	ground current		-200	-	mA
T_{stg}	storage temperature		-65	+150	$^{\circ}$ C
P_{tot}	total power dissipation	$T_{amb} = -40$ $^{\circ}$ C to +125 $^{\circ}$ C	[3] -	500	mW

[1] The minimum input voltage ratings may be exceeded if the input current ratings are observed.

[2] The output voltage ratings may be exceeded if the output current ratings are observed.

[3] Above 70 $^{\circ}$ C the value of P_{tot} derates linearly with 1.8 mW/K.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		1.65	-	3.6	V
		functional	1.2	-	-	V
V_I	input voltage		0	-	5.5	V
V_O	output voltage	output HIGH or LOW state	0	-	V_{CC}	V
		output 3-state	0	-	5.5	V
T_{amb}	ambient temperature	in free air	-40	-	+125	$^{\circ}$ C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 1.65$ V to 2.7 V	-	-	20	ns/V
		$V_{CC} = 2.7$ V to 3.6 V	-	-	10	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	
V _{IH}	HIGH-level input voltage	V _{CC} = 1.2 V	1.08	-	-	1.08	-	V
		V _{CC} = 1.65 V to 1.95 V	0.65 × V _{CC}	-	-	0.65 × V _{CC}	-	V
		V _{CC} = 2.3 V to 2.7 V	1.7	-	-	1.7	-	V
		V _{CC} = 2.7 V to 3.6 V	2.0	-	-	2.0	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 1.2 V	-	-	0.12	-	0.12	V
		V _{CC} = 1.65 V to 1.95 V	-	-	0.35 × V _{CC}	-	0.35 × V _{CC}	V
		V _{CC} = 2.3 V to 2.7 V	-	-	0.7	-	0.7	V
		V _{CC} = 2.7 V to 3.6 V	-	-	0.8	-	0.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}						
		I _O = -100 μA; V _{CC} = 1.65 V to 3.6 V	V _{CC} - 0.2	V _{CC}	-	V _{CC} - 0.3	-	V
		I _O = -2 mA; V _{CC} = 1.65 V	1.2	-	-	1.05	-	V
		I _O = -4 mA; V _{CC} = 2.3 V	1.8	-	-	1.65	-	V
		I _O = -6 mA; V _{CC} = 2.7 V	2.2	-	-	2.05	-	V
		I _O = -12 mA; V _{CC} = 3.0 V	2.2	-	-	2.0	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}						
		I _O = 100 μA; V _{CC} = 1.65 V to 3.6 V	-	-	0.2	-	0.3	V
		I _O = 2 mA; V _{CC} = 1.65 V	-	-	0.45	-	0.65	V
		I _O = 4 mA; V _{CC} = 2.3 V	-	-	0.6	-	0.8	V
		I _O = 6 mA; V _{CC} = 2.7 V	-	-	0.4	-	0.6	V
		I _O = 12 mA; V _{CC} = 3.0 V	-	-	0.55	-	0.8	V
I _I	input leakage current	V _{CC} = 3.6 V; V _I = 5.5 V or GND ^[2]	-	±0.1	±5	-	±20	μA
I _{OZ}	OFF-state output current	V _I = V _{IH} or V _{IL} ; V _{CC} = 3.6 V; V _O = 5.5 V or GND; ^[2]	-	±0.1	±5	-	±20	μA
I _{OFF}	power-off leakage supply	V _{CC} = 0 V; V _I or V _O = 5.5 V	-	±0.1	±10	-	±20	μA
I _{CC}	supply current	V _{CC} = 3.6 V; V _I = V _{CC} or GND; I _O = 0 A	-	0.1	40	-	160	μA
ΔI _{CC}	additional supply current	per input pin; V _{CC} = 2.7 V to 3.6 V; V _I = V _{CC} - 0.6 V; I _O = 0 A	-	5	500	-	5000	μA
C _I	input capacitance	V _{CC} = 0 V to 3.6 V; V _I = GND to V _{CC}	-	5.0	-	-	-	pF
I _{BHL}	bus hold LOW current	V _{CC} = 1.65 V; V _I = 0.58 V ^{[3][4]}	10	-	-	10	-	μA
		V _{CC} = 2.3 V; V _I = 0.7 V	30	-	-	25	-	μA
		V _{CC} = 3.0 V; V _I = 0.8 V	75	-	-	60	-	μA

Table 6. Static characteristics ...continued

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	
I _{BHH}	bus hold HIGH current	V _{CC} = 1.65 V; V _I = 1.07 V [3][4]	-10	-	-	-10	-	μA
		V _{CC} = 2.3 V; V _I = 1.7 V	-30	-	-	-25	-	μA
		V _{CC} = 3.0 V; V _I = 2.0 V	-75	-	-	-60	-	μA
I _{BHLO}	bus hold LOW overdrive current	V _{CC} = 1.95 V [3][5]	200	-	-	200	-	μA
		V _{CC} = 2.7 V	300	-	-	300	-	μA
		V _{CC} = 3.6 V	500	-	-	500	-	μA
I _{BHHO}	bus hold HIGH overdrive current	V _{CC} = 1.95 V [3][5]	-200	-	-	-200	-	μA
		V _{CC} = 2.7 V	-300	-	-	-300	-	μA
		V _{CC} = 3.6 V	-500	-	-	-500	-	μA

[1] All typical values are measured at V_{CC} = 3.3 V (unless stated otherwise) and T_{amb} = 25 °C.

[2] The bus hold circuit is switched off when V_I > V_{CC}, allowing 5.5 V on the input terminal.

[3] Valid for data inputs only. Note that control inputs do not have a bus hold circuit.

[4] The specified sustaining current at the data input holds the input below the specified V_I level.

[5] The specified overdrive current at the data input forces the data input to the opposite logic input state.

10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V). For test circuit see [Figure 6](#).

Symbol	Parameter	Conditions	T _{amb} = -40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	
t _{pd}	propagation delay	nAn to nYn; see Figure 4 [2]						
		V _{CC} = 1.2 V	-	11.0	-	-	-	ns
		V _{CC} = 1.65 V to 1.95 V	1.5	6.0	15.0	1.5	17.2	ns
		V _{CC} = 2.3 V to 2.7 V	1.0	3.2	7.4	1.0	8.2	ns
		V _{CC} = 2.7 V	1.0	3.3	6.7	1.0	8.5	ns
t _{en}	enable time	n $\overline{O}E$ to nYn; see Figure 5 [2]						
		V _{CC} = 1.2 V	-	15.0	-	-	-	ns
		V _{CC} = 1.65 V to 1.95 V	1.7	6.8	15.3	1.7	17.7	ns
		V _{CC} = 2.3 V to 2.7 V	1.5	3.8	8.0	1.5	8.9	ns
		V _{CC} = 2.7 V	1.5	4.2	7.6	1.5	9.5	ns
t _{dis}	disable time	n $\overline{O}E$ to nYn; see Figure 5 [2]						
		V _{CC} = 1.2 V	-	10.0	-	-	-	ns
		V _{CC} = 1.65 V to 1.95 V	2.2	3.9	8.2	2.2	9.5	ns
		V _{CC} = 2.3 V to 2.7 V	0.5	2.1	4.4	0.5	5.0	ns
		V _{CC} = 2.7 V	1.5	3.1	4.7	1.5	6.0	ns
		V _{CC} = 3.0 V to 3.6 V	1.5	2.8	4.5	1.5	6.0	ns

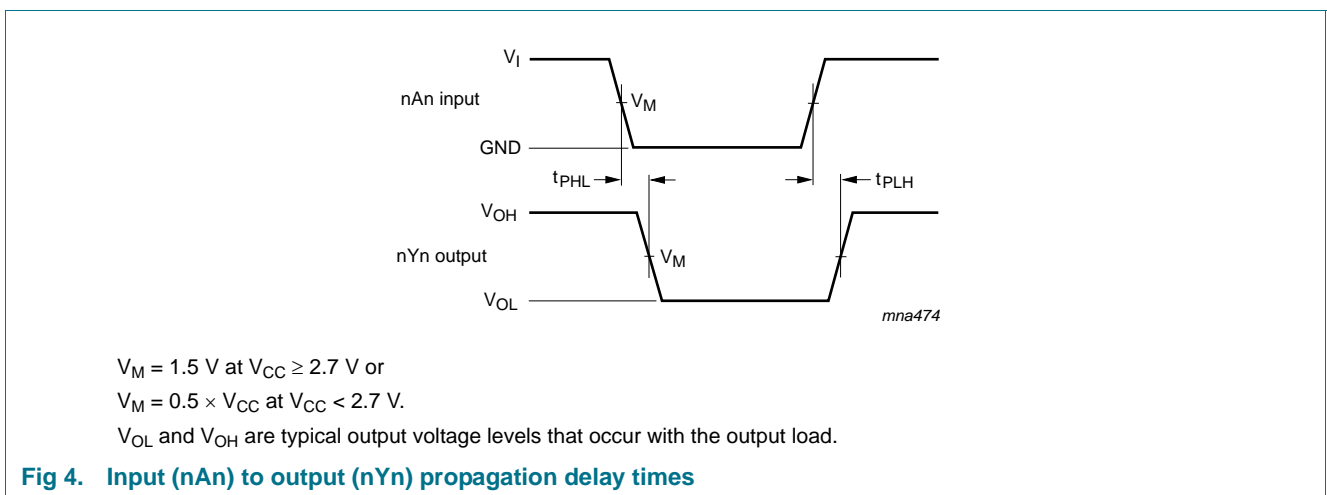
Table 7. Dynamic characteristics ...continued

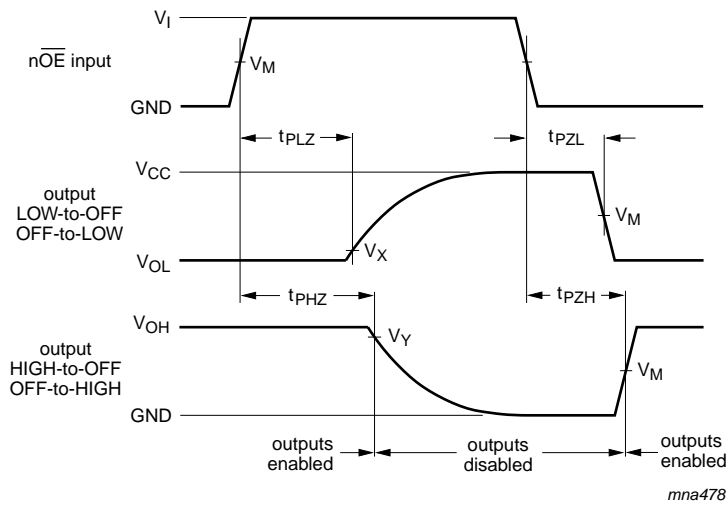
Voltages are referenced to GND (ground = 0 V). For test circuit see [Figure 6](#).

Symbol	Parameter	Conditions	T _{amb} = -40 °C to +85 °C			-40 °C to +125 °C		Unit	
			Min	Typ ^[1]	Max	Min	Max		
t _{sk(o)}	output skew time	V _{CC} = 3.0 V to 3.6 V	[3]	-	-	1.0	-	1.5	ns
C _{PD}	power dissipation capacitance	per flip-flop; V _I = GND to V _{CC}	[4]						
		outputs enabled							
		V _{CC} = 1.65 V to 1.95 V		-	4.8	-	-	-	pF
		V _{CC} = 2.3 V to 2.7 V		-	8.3	-	-	-	pF
		V _{CC} = 3.0 V to 3.6 V		-	11.4	-	-	-	pF

- [1] Typical values are measured at T_{amb} = 25 °C and V_{CC} = 1.2 V, 1.8 V, 2.5 V, 2.7 V, and 3.3 V respectively.
- [2] t_{pd} is the same as t_{PLH} and t_{PHL}.
t_{en} is the same as t_{PZL} and t_{PZH}.
t_{dis} is the same as t_{PLZ} and t_{PHZ}.
- [3] Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.
- [4] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
P_D = C_{PD} × V_{CC}² × f_i × N + Σ(C_L × V_{CC}² × f_o) where:
f_i = input frequency in MHz; f_o = output frequency in MHz
C_L = output load capacitance in pF
V_{CC} = supply voltage in Volts
N = number of inputs switching
Σ(C_L × V_{CC}² × f_o) = sum of the outputs

11. AC waveforms





$V_M = 1.5 \text{ V}$ at $V_{CC} \geq 2.7 \text{ V}$;

$V_M = 0.5 \times V_{CC}$ at $V_{CC} < 2.7 \text{ V}$.

$V_X = V_{OL} + 0.3 \text{ V}$ at $V_{CC} \geq 2.7 \text{ V}$ or

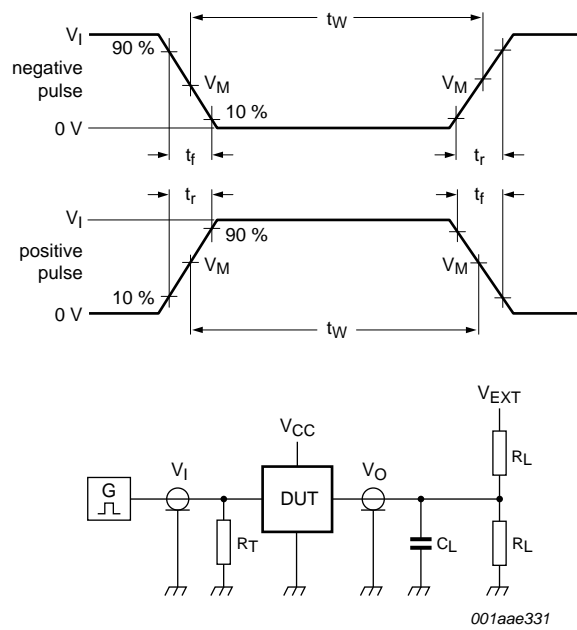
$V_X = V_{OL} + 0.1 \text{ V}$ at $V_{CC} < 2.7 \text{ V}$.

$V_Y = V_{OH} - 0.3 \text{ V}$ at $V_{CC} \geq 2.7 \text{ V}$ or

$V_Y = V_{OH} - 0.1 \text{ V}$ at $V_{CC} < 2.7 \text{ V}$.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 5. 3-state enable and disable times



Test data is given in [Table 8](#).

Definitions for test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

V_{EXT} = External voltage for measuring switching times.

Fig 6. Load circuitry for switching times

Table 8. Test data

Supply voltage	Input		Load		V_{EXT}		
	V_I	t_r, t_f	C_L	R_L	t_{PLH}, t_{PHL}	t_{PLZ}, t_{PZL}	t_{PHZ}, t_{PZH}
1.2 V	V_{CC}	≤ 2 ns	30 pF	1 kΩ	open	$2 \times V_{CC}$	GND
1.65 V to 1.95 V	V_{CC}	≤ 2 ns	30 pF	1 kΩ	open	$2 \times V_{CC}$	GND
2.3 V to 2.7 V	V_{CC}	≤ 2 ns	30 pF	500 Ω	open	$2 \times V_{CC}$	GND
2.7 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	$2 \times V_{CC}$	GND
3.0 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	$2 \times V_{CC}$	GND

12. Package outline

LFBGA96: plastic low profile fine-pitch ball grid array package; 96 balls; body 13.5 x 5.5 x 1.05 mm SOT536-1

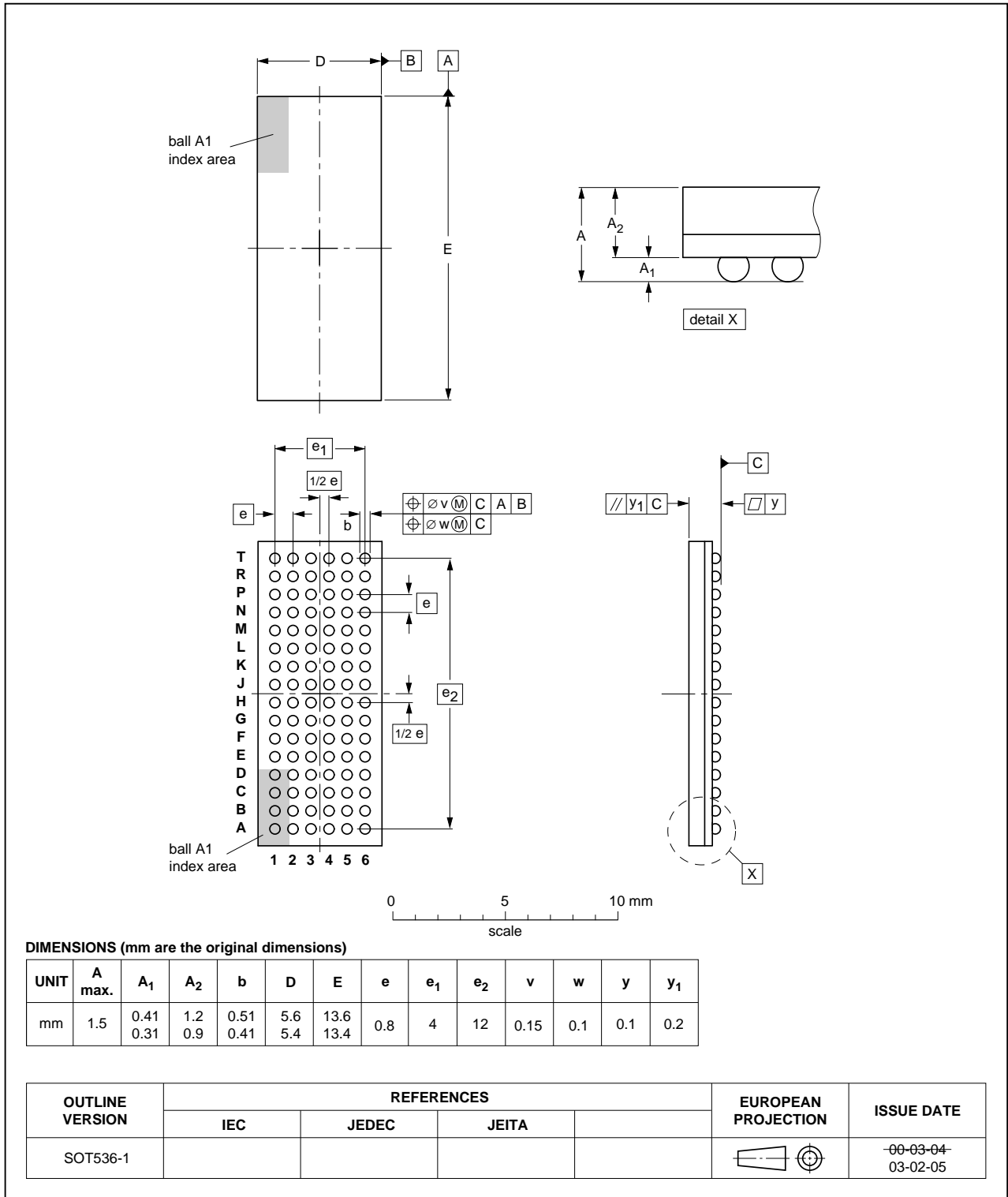


Fig 7. Package outline SOT536-1 (LFBGA96)

13. Abbreviations

Table 9. Abbreviations

Acronym	Description
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

14. Revision history

Table 10: Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVCH322244A v.3	20111216	Product data sheet	-	74LVCH322244A v.2
Modifications:	<ul style="list-style-type: none"> The format of this document has been redesigned to comply with the new identity guidelines of NXP Semiconductors. Legal texts have been adapted to the new company name where appropriate. Table 4, Table 5, Table 6, Table 7 and Table 8: values added for lower voltage ranges. 			
74LVCH322244A v.2	20040519	Product specification	-	74LVCH322244A v.1
74LVCH322244A v.1	19991124	Product specification	-	-

15. Legal information

15.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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