Features

- **Multiband Transceiver: 400 MHz to 950 MHz**
- **Monochip RF Solution: Transmitter-Receiver-Synthesizer**
- **Integrated PLL and VCO: No External Coil**
- **Very Resistant to Interferers by Design**
- **Digital Channel Selection**
- **200 Hz Steps**
- **Data Rates up to 64 kbps with Data Clock and no Manchester Encoding Required**
- **High Output Power Allowing Very Low Cost Printed Antennas:**
  - **+10 dBm in the 915 MHz Frequency Band**
  - **+12 dBm in the 868 MHz Frequency Band**
  - **+14 dBm in the 433 MHz Frequency Band**
- **FSK Modulation: Integrated Modulator and Demodulator**
- **Power Savings:**
  - **Stand Alone "Sleep" Mode and "Wake-up" Procedures**
  - **8 Selectable Digital Levels for Output Power**
  - **High Data Rate and Fast Settling Time of the PLL**
  - **Oscillator Running Mode "Ready to Start"**
  - **Analog FSK Discriminator Allowing Measurement and Correction of Frequency Drifts**
- **100% Digital Interface through R/W Registers Including:**
  - **Digital RSSI**
  - **V_{CC} Readout**

Description

The AT86RF211 (aka: TRX01) is a single chip transceiver dedicated to low power wireless applications, optimized for licence-free ISM band operations from 400 MHz to 950 MHz. Its flexibility and unique level of integration make it a natural choice for any system related to telemetry, remote controls, alarms, radio modems, Automatic Meter Reading, hand held terminals, high-tech toys, etc. The AT86RF211 makes bidirectional communications affordable for applications such as secured transmissions with hand-shake procedures, new features and services, etc. The AT86RF211 can easily be configured to provide the optimal solution for the user's application: choice of external filters vs. technical requirements (bandwidth, selectivity, immunity, range, etc), and software protocol (single channel, multiple channel, FHSS). The AT86RF211 is also well adapted to battery operated systems, as it can be powered with only 2.4V. It also offers a "Wake Up" receiver feature to save power by alerting the associated microcontroller only when a valid inquiry is detected.

FSK Transceiver for ISM Radio Applications

AT86RF211 (aka: TRX01)

Smart RF

General Overview

General Overview of Functioning

The AT86RF211 is a microcontroller RF peripheral: all the user has to do is to write/read registers to setup the chip (i.e. frequency selection) or have information about parameters such as RSSI level, Vbattery, PLL lock state. All these operations are carried out via a three-wire serial interface.

Normal Mode

The chip is set-up by the microcontroller: frequency and mode (Rx or Tx). Then it acts like a "pipe": any data entering DATAMSG is immediately radiated (Tx) or any wanted signal collected by the aerial is demodulated, transferred to the microcontroller by the same pin DATAMSG (Rx) as reshaped bits. No data is stored or processed into the chip. See Figure 1.

Note: In Rx mode, a clock recovery DATACLK is available on the digital interface to provide the microcontroller with a synchronization signal.

Wake-up Mode

The chip is set up in a special Rx mode called sleep mode. The chip wakes up periodically thanks to its internal timer (stand alone procedure, the microcontroller is in power-down mode), waiting for an expected message previously defined. If no correct sequence is received, the periodic scan continues.

If a correct message is detected, its data field is stored into the AT86RF211 (up to 32 bits) and an interrupt is generated on the WAKEUP pin.

See Figure 2 and Figure 3.
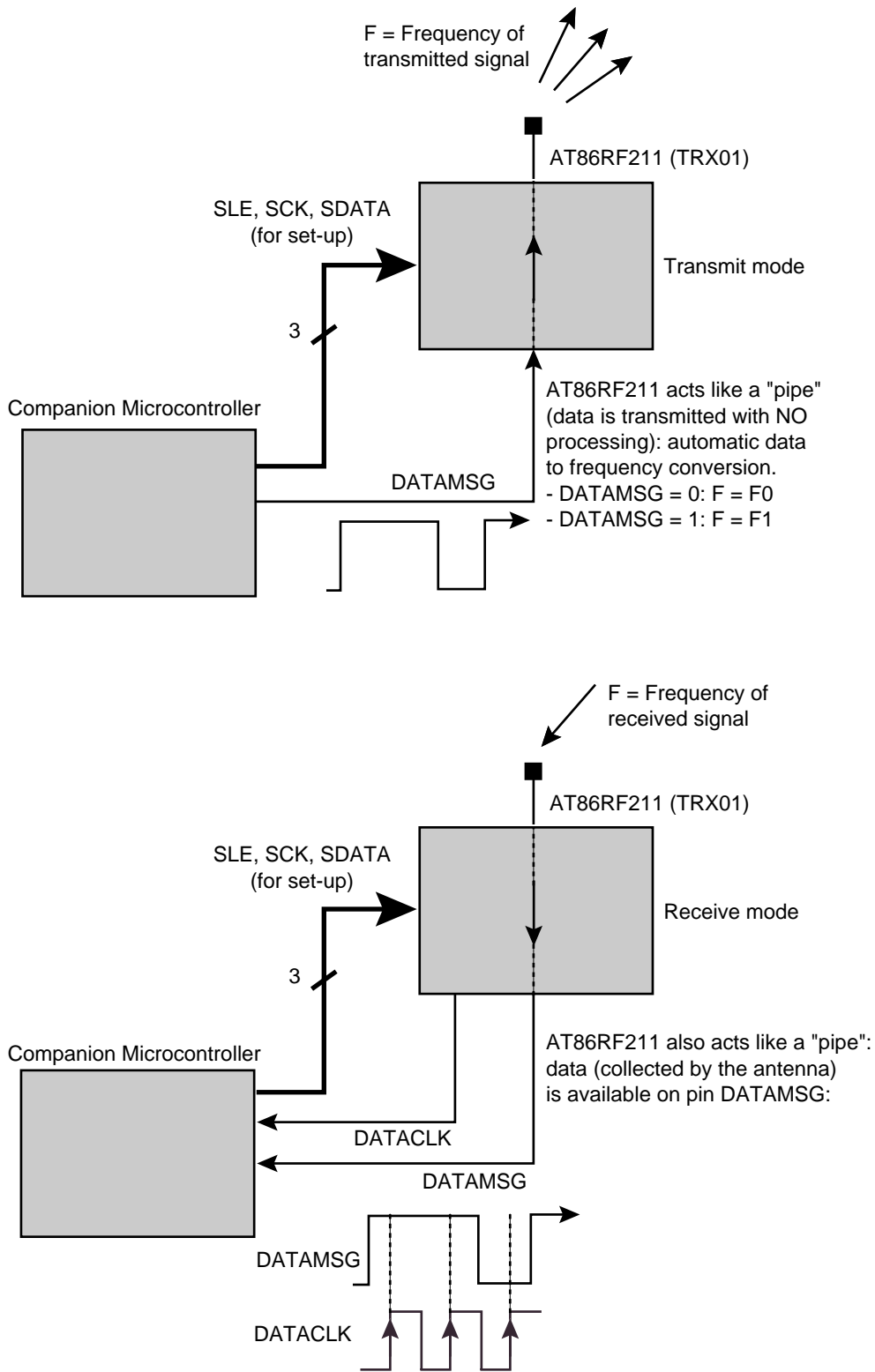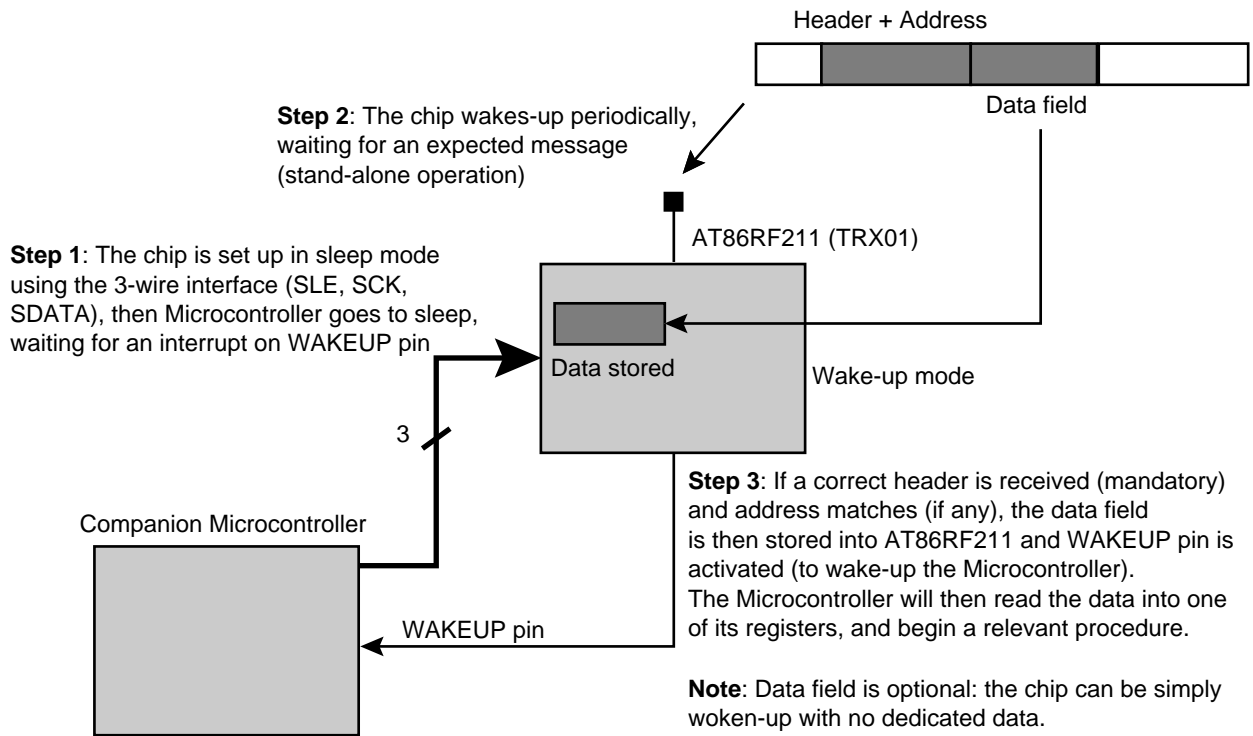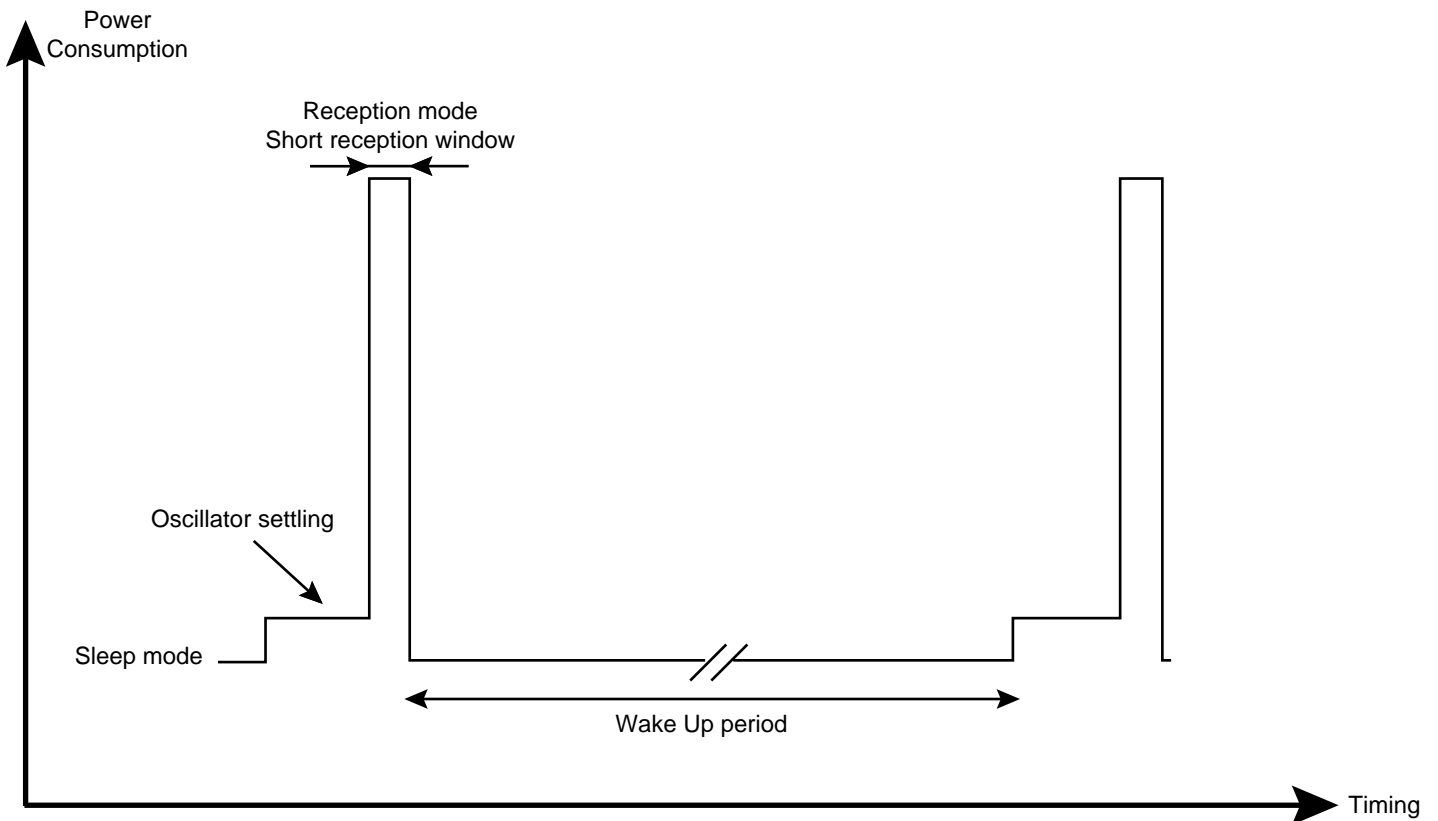
Figure 1. Reception and Transmit Mode

F = Frequency of transmitted signal

AT86RF211 (TRX01)

SLE, SCK, SDATA (for set-up)

Transmit mode

3

Companion Microcontroller

DATAMSG

AT86RF211 acts like a "pipe" (data is transmitted with NO processing): automatic data to frequency conversion.
- DATAMSG = 0: F = F0
- DATAMSG = 1: F = F1

F = Frequency of received signal

AT86RF211 (TRX01)

SLE, SCK, SDATA (for set-up)

Receive mode

3

Companion Microcontroller

DATACLK

DATAMSG

AT86RF211 also acts like a "pipe": data (collected by the antenna) is available on pin DATAMSG:

DATAMSG

DATACLK

Figure 2. Wake-up Overview

Header + Address

Data field

Step 2: The chip wakes-up periodically, waiting for an expected message (stand-alone operation)

AT86RF211 (TRX01)

Step 1: The chip is set up in sleep mode using the 3-wire interface (SLE, SCK, SDATA), then Microcontroller goes to sleep, waiting for an interrupt on WAKEUP pin

Data stored

Wake-up mode

3

Companion Microcontroller

Step 3: If a correct header is received (mandatory) and address matches (if any), the data field is then stored into AT86RF211 and WAKEUP pin is activated (to wake-up the Microcontroller). The Microcontroller will then read the data into one of its registers, and begin a relevant procedure.

Note: Data field is optional: the chip can be simply woken-up with no dedicated data.

WAKEUP pin

Figure 3. Periodical Scan

Power Consumption

Reception mode
Short reception window

Oscillator settling

Sleep mode

Wake Up period

Timing

Block Diagram

Figure 4. AT86RF211 Block Diagram
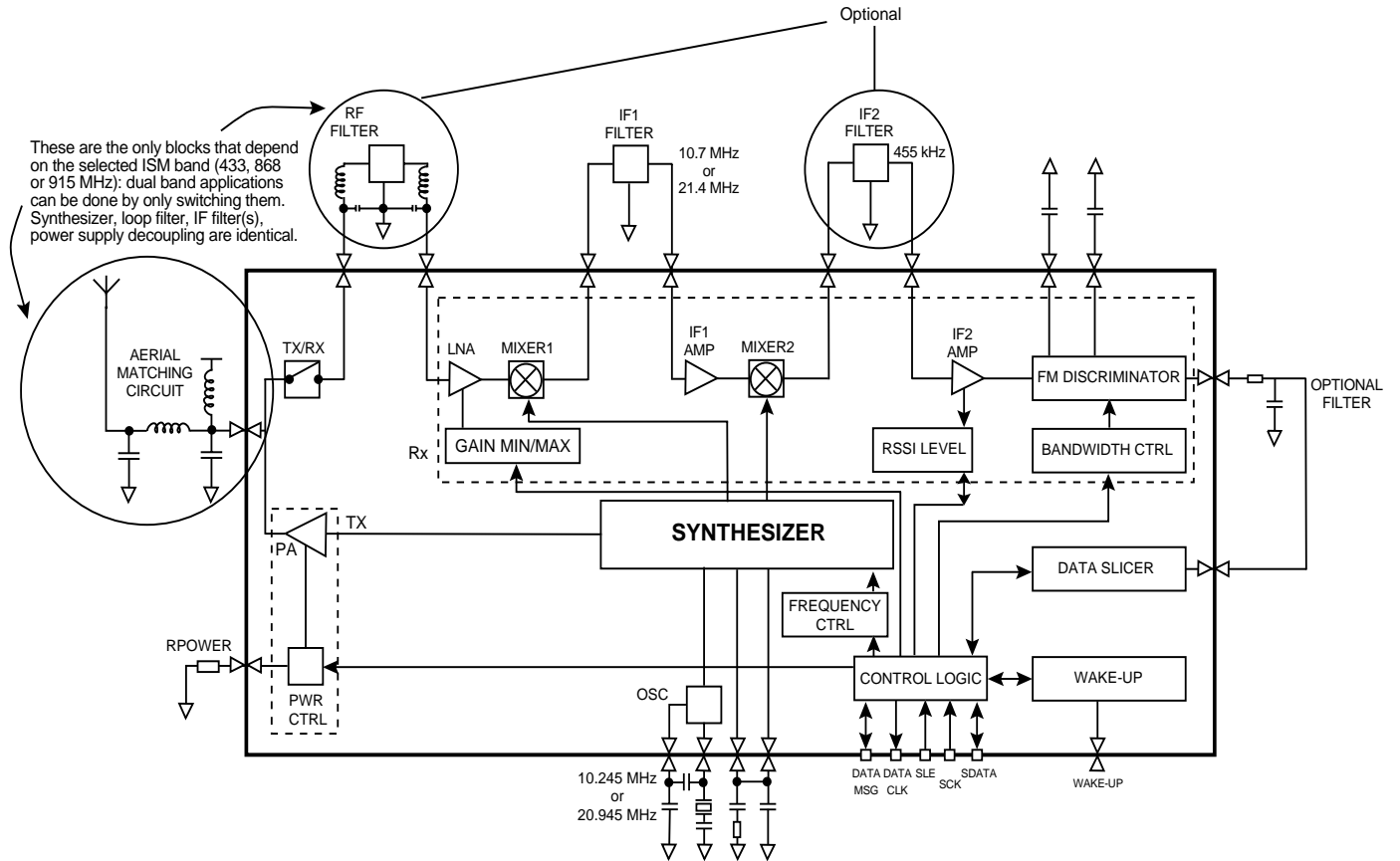
Pin Description

Table 1. Pinout

Pin	Name	Comments	Pin	Name	Comments
1	RPOWER	Full scale output power resistor	25	SKFILT	Threshold for data slicer
2	TXGND1	GND	26	DSIN	Data slicer input
3	RF	RF input/output	27	DISCOUT	Discriminator output
4	TXGND2	GND	28	IF2VCC	VCC
5	TXGND3	GND	29	IF2GND	GND
6	TXGND4	GND	30	IF2IN	IF2 amplifier input
7	TXVCC	VCC	31	IF2DEC	2.2 nF to ground
8	TXGND5	GND	32	DISCFILT	Discriminator bypass
9	DIGND	GND	33	IF2OUT	IF2 mixer output
10	DIVCC	VCC	34	IF1DEC	4.7 nF to ground
11	DATAMSG	Input/output digital message	35	IF1IN	IF1 amplifier input
12	SLE	Serial interface enable	36	IF1OUT	IF1 mixer output
13	SCK	Serial interface clock	37	AGND	GND
14	SDATA	Serial interface data	38	AVCC	VCC
15	WAKEUP	Wake-up output	39	CVCC2	VCC
16	DATACLK	Data clock recovery	40	CGND2	GND
17	–	Test pin: do not connect	41	FILT1	Synthesizer output
18	EVCC1	VCC	42	VCOIN	Synthesizer input (VCO)
19	EGND1	GND	43	EVCC2	VCC
20	–	Test pin: do not connect	44	EGND2	GND
21	CGND1	GND	45	RXIN	LNA input from SAW filter
22	CVCC1	VCC	46	RXVCC	VCC
23	XTAL1	Crystal input	47	RXGND	GND
24	XTAL2	Crystal output	48	SWOUT	Switch output

Notes: 1. All V_{CC} pins must be connected in each functional mode (Tx, Rx, wake-up, PDN)
2. To be connected:
Rx mode only, all but: 1, 3, 17, 20, 48
Tx mode only, all but: 15 to 17, 20, 25 to 27, 30 to 36, 45, 48
3. Pin 20 must remain unconnected or connected to ground

Detailed Description

Frequency Synthesis

Crystal Reference Oscillator   The reference clock is based on a classical Colpitts architecture with three external capacitors.

An XTAL with load capacitor in the range of 10 pF - 20 pF is recommended. The bias circuitry of the oscillator is optimized to produce a low drive level for the XTAL. This reduces XTAL aging. Any standard, parallel mode 10.245 MHz or 20.945 MHz crystal can be used.

Note: The PLL is activated only when the oscillator is stabilized.

Figure 5. Crystal Oscillator Inputs
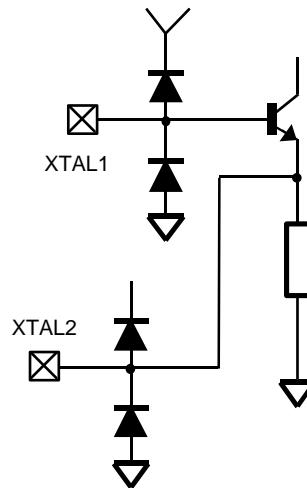
Figure 6. Typical Networks
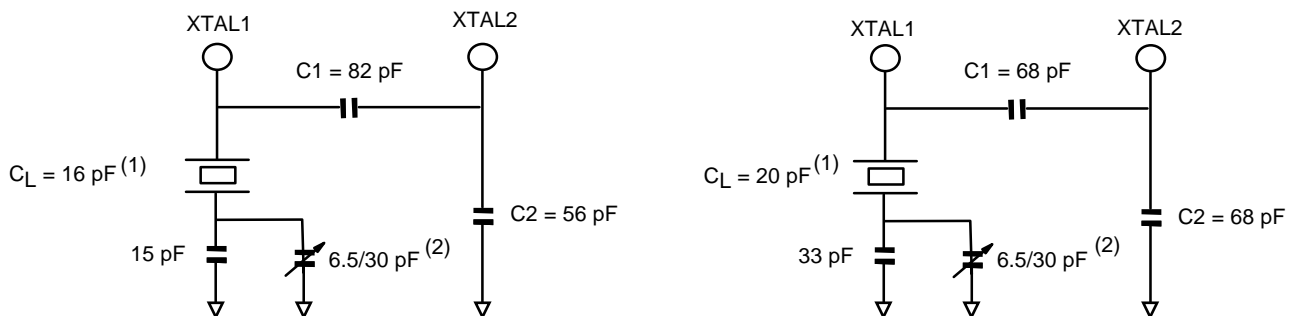
Notes: 1. Various load capacitance (C_L) crystals can be used. In case C_L differs of 16 pF or 20 pF, the surrounding network (C1, C2) must be re-calculated.
2. Thanks to the fine steps of the synthesizer (200 Hz), the trimmer capacitor can be replaced by a software adjustment.

Synthesizer   A high-speed, high-resolution multi-loop synthesizer is integrated. The synthesizer can operate within two frequency bands: 400 MHz to 480 MHz and 800 MHz to 950 MHz. All channels in these two bands can be selected through software programming (registers F0 to F3). All circuitry is on-chip with the exception of the PLL loop filter. The phase comparison is made thanks to a charge pump topology. Typical charge pump current is 225 µA.

Figure 7. Synthesizer Loop Filter Schematic
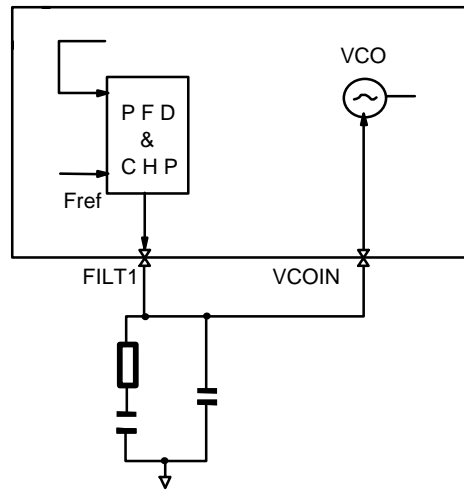
Note: The PLL loop filter can be designed to optimize the phase noise around the carrier.
Three configurations can be suggested, regarding the application and channel spacing:
- Narrow band: (14.7 kΩ + 2.2 nF) // 220 pF
- Typical: (3.3 kΩ + 5.6 nF) // 560 pF
- High datarates: (10 kΩ + 1 nF) // 100 pF

Receiver Description

Figure 8. Typical Expected Currents in Rx Mode

Supply Current - Rx Mode

Detailed Current - Rx Mode
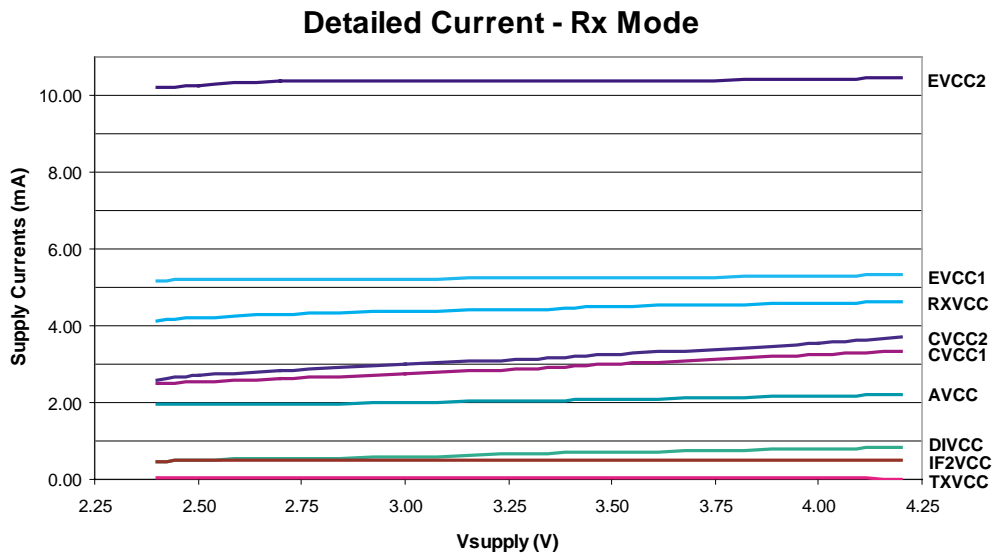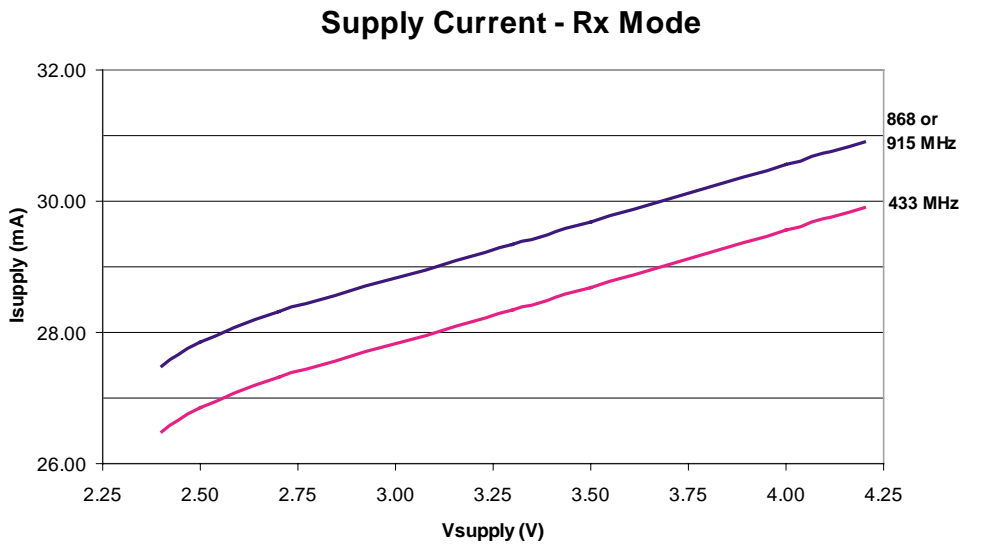
Overview and Choice of Intermediate Frequencies

For selectivity and flexibility purpose, a classical and robust 2 IF superheterodyne architecture has been selected for the AT86RF211. In order to minimize the external components cost, the most popular IF values have been chosen. The impedances of the input/output of the mixing stages have been internally matched to the most usual ceramic filter impedances.

Two typical IF values are suggested:

- 10.7 MHz is the most popular option.
- 21.4 MHz: the image frequency is far enough from the carrier frequency to enable the use of a front-end ceramic filter instead of a SAW filter. It is also noticeable that 21.4 MHz quartz filters usually have more abrupt slopes than 10.7 MHz ceramic filters.

Rx - Tx Switch

A SPST switch is integrated. In the transmission mode, it protects the LNA input from the large voltage swings of the PA output (up to several volts peak-to-peak), which is switched to a high impedance state. It is automatically turned ON or OFF by the RX/TX control bit. The insertion loss is about 2 dB and the reverse isolation about 30 dB in a 300Ω environment.

Image Rejection and RF Filter

The immunity of the AT86RF211 can be improved with an external band-pass filter.

For example, when using a SAW Filter, this device must be matched with the LNA input and the switch output. The following scheme gives the typical implementation for an 868 MHz application with a 50Ω/50Ω SAW filter.

Figure 9. Typical 50Ω SAW Filter Implementation in the 868 MHz Band
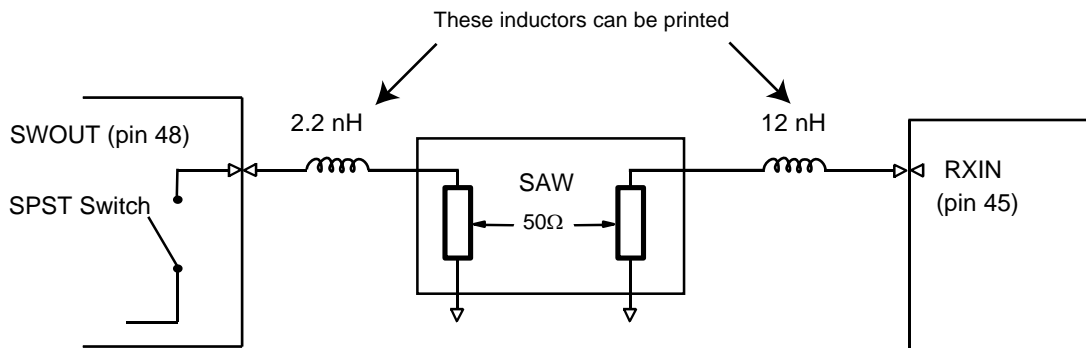
See Table 2 for precise matching information.

The SAW filter can be replaced by a TEM ceramic, helicoidal or a ceramic coax λ/4 resonator designed as a narrow band-pass filter. For instance, with an IF selected at 10.7 MHz, a -3 dB bandwidth of 5 MHz, with an insertion loss of 1 dB and an image rejection of 12 dB can be achieved with the following:

Figure 10. TEM Filter
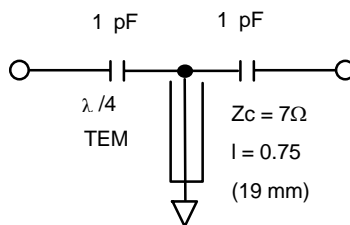
Such a filter also provides an out-of-band interference rejection greater than 20dB, 40 MHz away from 433 MHz.

First LNA/Mixer

The main characteristics of the LNA/Mixer are typically:

- Voltage gain: 17 dB for the LNA/Mixer; 11 dB if gain min. is selected
- Bandwidth: 1.2 GHz
- Noise figure of LNA alone: 3 dB at 900 MHz, best matching
- Noise figure of LNA + mixer:
  8 dB at 900 MHz, with maximum gain and best matching
  12 dB at 900 MHz, with minimum gain and best matching
- 1 dB compression point: -20 dBm at the input of LNA
- Matching:

Table 2. Matching Information

Frequency Band	RXIN[1]	SWOUT[2]
433 MHz	$35 + j\,170\Omega$	$24 - j\,43\Omega$
868 MHz	$37 + j\,85\Omega$	$50 - j\,42\Omega$
915 MHz	$30 + j\,85\Omega$	$50 - j\,42\Omega$

Notes: 1. RXIN: impedance to be seen by LNA input for NF optimization purpose
        2. SWOUT: output impedance of the RF switch

The gain is programmable through bit 25 of CTRL1 register (6dB attenuation when min gain is selected). The choice for the matching between the SWITCH and the LNA depends mainly on the chosen SAW filter. Usually in/out impedance of SAW filters is 50Ω, but other ones can be implemented and the matching network recalculated thanks to the previous impedance table.

The LNA is directly coupled to the first mixer. Input and output of the LNA/Mixer must be connected through a capacitive link because of their internal DC coupling. A SAW or ceramic filter provides such a link.
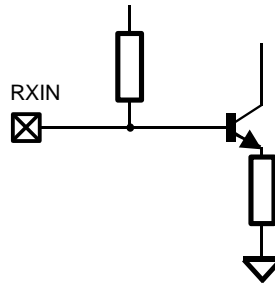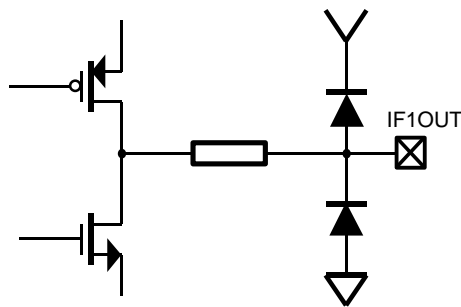
Figure 11. Schematic Input of the LNA

Figure 12. Schematic Output of the Mixer

The first mixer translates the input RF signal down to 10.7 MHz or 21.4 MHz as chosen by the user. The local oscillator is provided by the same synthesizer which will generate a local frequency 10.7 MHz or 21.4 MHz away from the Tx carrier frequency.

The output impedance of the mixer is 330Ω with a 20% accuracy, so that low cost, standard 10.7 MHz ceramic filters can be directly driven. Other IFs may be chosen thanks to the high bandwidth (50 MHz) of the mixer.

IF1 filtering

A popular ceramic filter is used to reject the second image frequency and provide a first level of filtering.

The IF1 filter can however be removed; it leads to a sensitivity reduction of about 3 dB (the substitution coupling capacitor should be > 100 pF).

IF1 Gain and Second Mixer

The input impedance of the IF1 amplifier is naturally 330Ω to match the input filter. The voltage gain, i.e. gain at 10.7 MHz or 21.4 MHz added to the conversion gain at 455 kHz is typically 14 dB when loaded by 1700Ω. The second mixer operates at a fixed LO frequency of 10.245 MHz or 20.945 MHz. Its output impedance is 1700Ω in parallel with 20 pF.
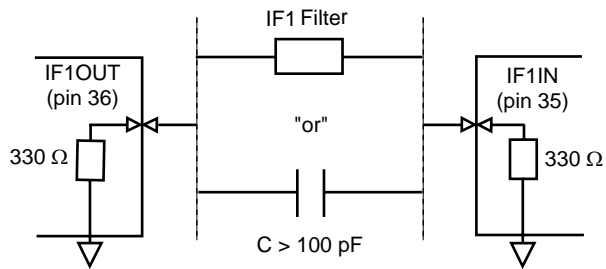
Figure 13. IF1 Filtering

Figure 14. Schematic Input of IF1 Amplifier
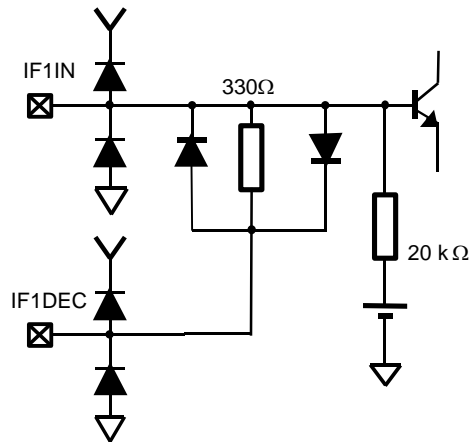
Figure 15. Schematic Output of the Second Mixer
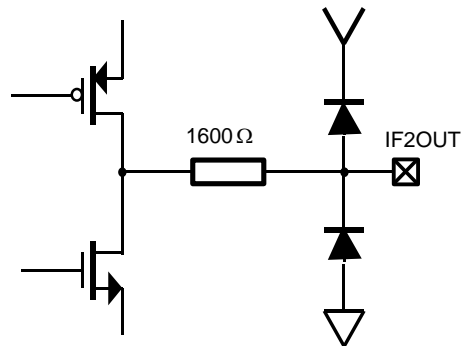
IF2 Filtering and Gain

IF2 filtering achieves a narrow channel selection. In case it is not used, it should be replaced by a > 1 nF coupling capacitor, thus the IF1 filter is the only part achieving the channel selection. Available commercial filters with a 35 kHz BW allow data rates up to 19.6 kbps if crystal temperature drifts are very low.

For faster communications and/or wider channelization, this ceramic filter can be replaced by an LC band-pass filter as proposed hereafter.

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Figure 16. LC Band-pass Filter
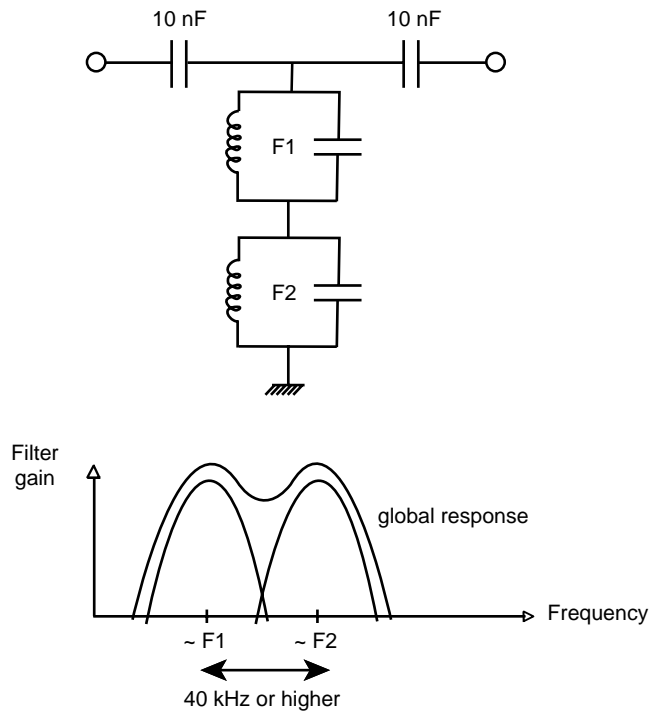
- 10 nF capacitors cut DC response forward and backward.
- The first network has the low cut-off frequency.
- The second network has the high cut-off frequency.

IF2 Amplifier Chain

The input impedance of the IF2 amplifier is 1700Ω. This value enables the use of popular filters with impedance between 1500Ω and 2000Ω. It is directly connected to the FSK demodulator. The bandwidth is internally limited to 1 MHz to minimize the noise before the discriminator. It acts like a band pass filter centered at 455 kHz with capacitive coupling between stages of amplifier and mixer. Total voltage gain is typically 86 dB. Thanks to the capacitive coupling, no slow DC feedback loop is needed enabling a fast turn on time. IF2DEC has to be decoupled with at least 2.2 nF.

Figure 17. Input of the IF2 Amplifier Schematic

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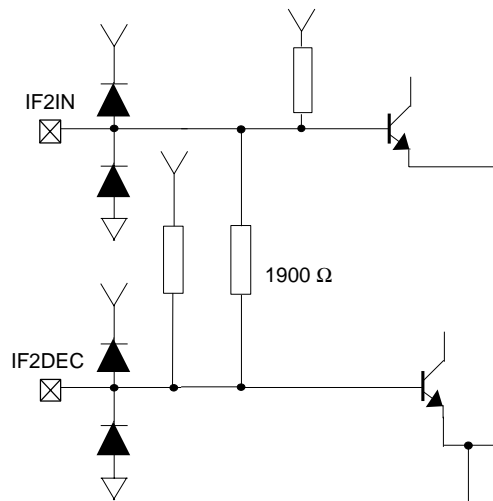
RSSI Output

The RSSI value can be read as a 6 bits word in the STATUS register. Its value is linear in dB as plotted below:

Figure 18. Typical RSSI output (board implementation, T = 25°C, V_{CC} = 3V)

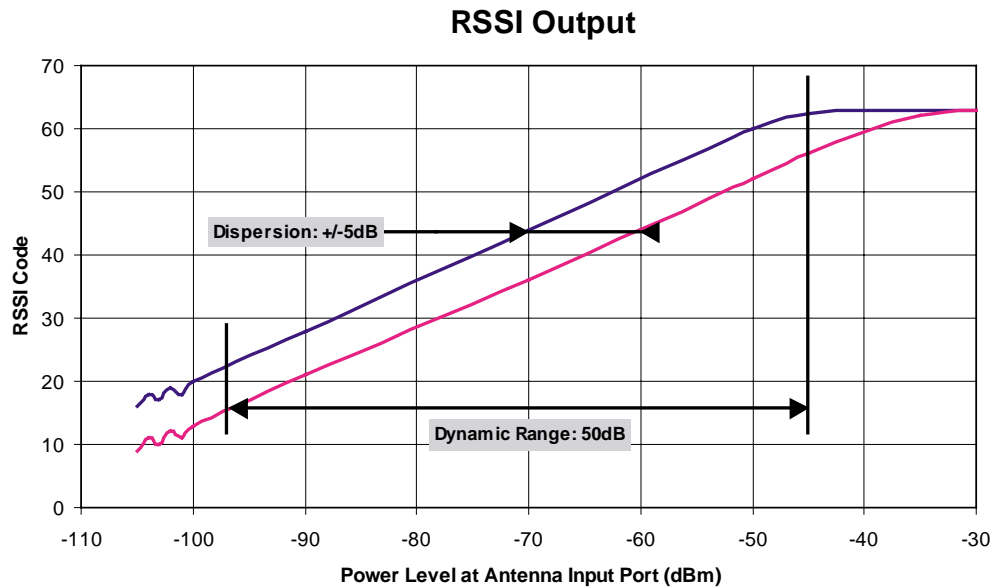Note: Should the RSSI be required for accurate measurement purpose (precision better than 5 dB), then it is possible to measure one value with a calibrated RF source and store it into the microcontroller, during the production testing.

The RSSI dynamic range is 50 dB from -95 dBm to -45 dBm RF input signal power, over temperature and power supply ranges. The RSSI LSB's value weighs about 1.3 dB in the linear area. The RSSI value is measured from the IF2 chain.

The RSSI is periodically measured thanks to a successive approximation ADC with a 12 µs clock. Thereafter, the time needed to complete the right code depends on the power step: a 10 dB step on the aerial leads to a 10/1.3 = 8 clock cycles, i.e. 96 µs (full range from code 0 to 63 = 756 µs). Its value can be compared with a user predefined value (TRSSI), so that the demodulated data is enabled only if the RSSI value is above this threshold. Some hysteresis effect may be added (see CTRL1 register's content).

The AT86RF211 also has the possibility to measure another voltage. The ADC measuring the RSSI can be turned into voltage or discriminator output DC level measurement.

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Figure 19. ADC Converter Input Selection
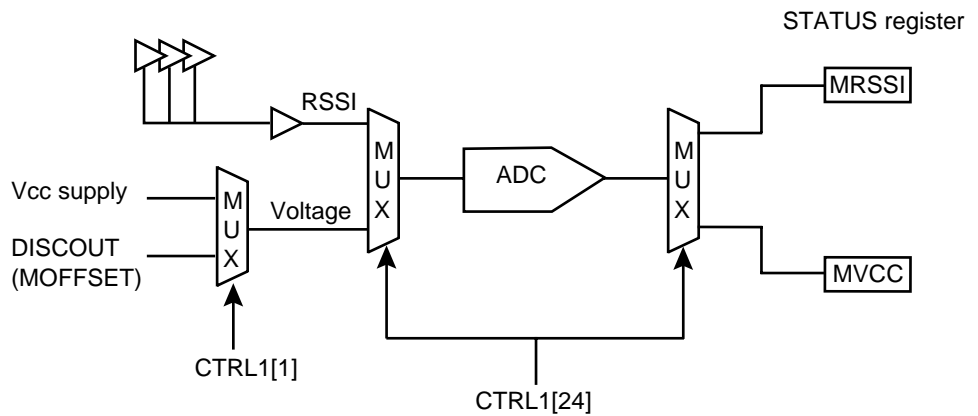
Note: For voltage measurement, the LSB weighs 85 mV and the reference voltage is 1.25V.

The ADC measuring the RSSI can be turned into voltage or discriminator output DC level measurement.

FSK Demodulator   Its structure is based on an oscillator:

Figure 20. Schematic of the FSK demodulator
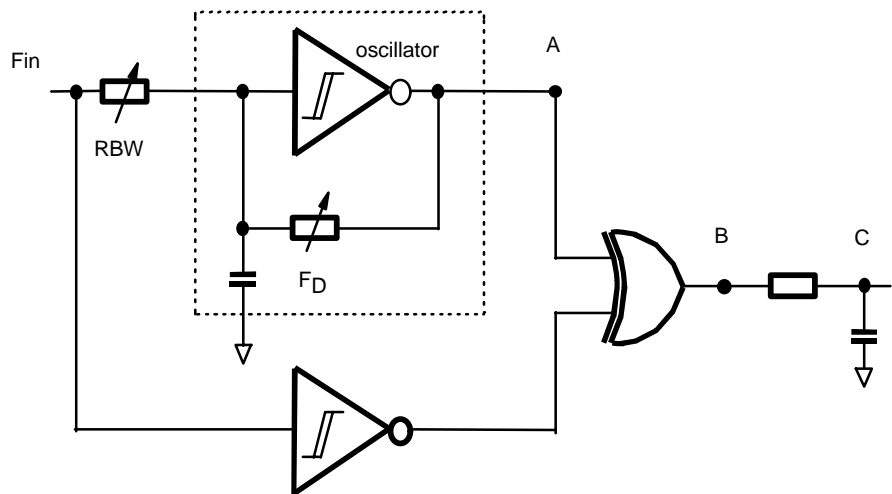
The oscillator's natural frequency is F_D and it actually oscillates at the Fin frequency. The signal at the output of the oscillator (point A) is proportional to the frequency difference between Fin and F_D. The XOR function translates the difference into a pulse duty cycle (point B).Thereafter by low-pass filtering of the signal is obtained a mean voltage of the signal (point C).

The architecture of this demodulation is thereby analog and allows the transmission of continuous data stream of the same value as the output voltage is proportional to the input frequency. Thus it is not mandatory to use Manchester encoding and the first bit is correctly demodulated.

The oscillator feedback resistor controls the center frequency F_D. It is adjusted according to the output of a dummy FSK demodulator driven by a 455 kHz internal reference frequency which is a division of the reference crystal. The discrete components connected to pin 32 DISCFILT are the loop filter of the PLL stabilizing the 455 kHz signal.

The input RBW resistor controls the discriminator bandwidth. This bandwidth is selected by CTRL1[6]. The default value is "standard discriminator BW". The slope of the discriminator increases by 5 mV/kHz/V with V_{CC} and is 14 mV at 2.4V.

Example:
V_{CC} = 3V implies +17 mV/kHz sensitivity for the demodulator
V_{CC} = 3.6V implies +20 mV/kHz sensitivity for the demodulator

Data Slicer

The analog signals at the output of the discriminator (DISCOUT, pin 27) are converted into CMOS level data by a high resolution comparator called a Data Slicer.

The Data Slicer has a reference for its comparator which can be chosen thanks to CTRL1[4]. The reference sets the comparison level of the comparator. One option is to extract the average value of the demodulated signal on the SKFILT pin (25), this is the external mode. The other option is to set an absolute value for this reference (internal mode).

• External mode:

The external mode uses the average value of the demodulated signal as the comparison level for the comparator. Thus there must be enough transitions in the message to ensure that the average value remains between the "0" level and the "1" level. Manchester encoding can be used in this mode as well as DC-free encoding schemes. The choice for SKFILT capacitor is a trade-off between the maximum duration of a constant bit (whatever "0" or "1") and the max allowed settling time to charge this capacitor after powering up.

Note: The SKFILT pin is in high impedance state during the "sleep" period of the Wake Up mode, so that the level is kept constant and there is no need to charge again this tank.

• Internal mode:

The internal mode uses the output of a DAC as the comparison level. Once this threshold has been correctly set, an "absolute" data slicing of the demodulated signal is possible: no need for DC-free modulation scheme (it is possible to send a "0" or "1" infinitely).

Figure 21. Schematic of the Data Slicer
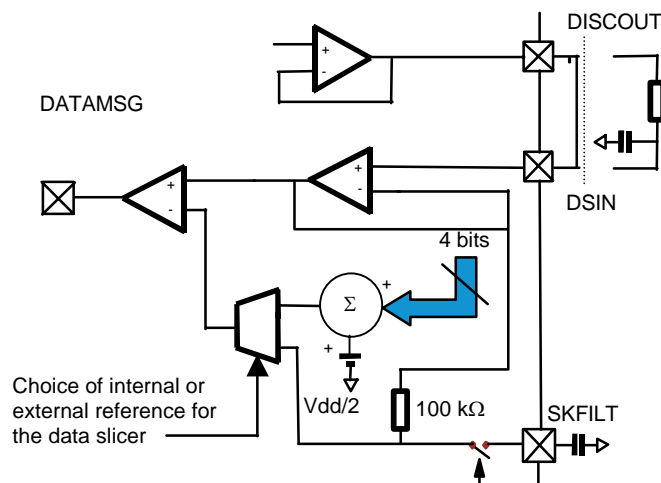
To operate this way, the user must make sure that the "0" and "1" level at the output of the discriminator are "on both sides" of the comparison level in order for the decision to be made properly.

Figure 22. How to Set Up the Data Slicing Parameters
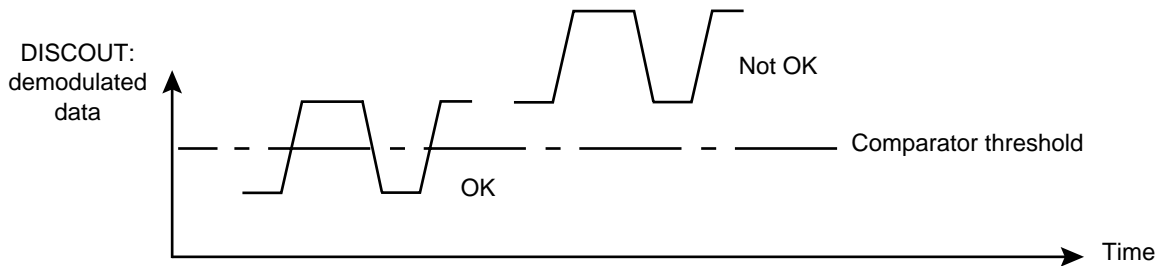
To set the discriminator and the Data Slicer accordingly:

- It is possible to measure the output DC level of the discriminator DISCOUT (thanks to the A/D embedded converter)
- DTR[1:0] make it possible to shift (up or down) the DC level at the output of the discriminator :
  - DTR[1] = 1: +180 mV + 77x (V_{CC} - 2.4V)
  - DTR[0] = 1: -180 mV - 77x (V_{CC} - 2.4V)
- DTR[5:2] make it possible to tune the comparison threshold around $V_{CC}/2$. 16 levels are possible, with a LSB = 15 mV per Volt of supply voltage. $V_{CC}/2$ corresponds to DTR[5:2] = 0111, and the RESET value is 1000.

These procedures can be made automatically by software. Please refer to the application note.

Transmitter Description

Figure 23. Typical Expected Currents in Tx Mode

Supply Current - Tx Mode

Detailed Current - Tx Mode
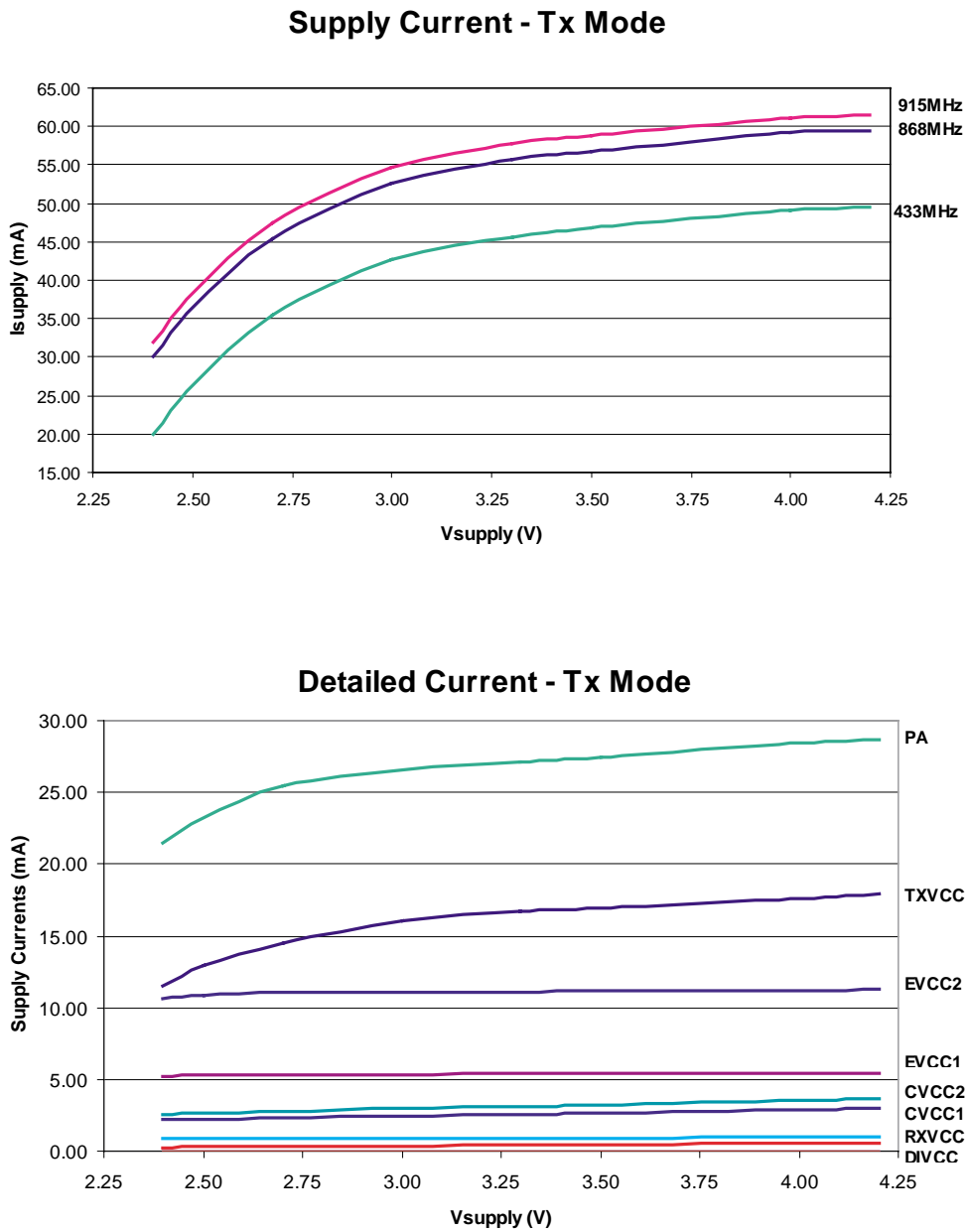
Power Amplification

The Power Amplifier has been built to deliver more than +10 dBm, i.e. 10 mW in the three popular frequency bands. This power level is intended to be measured on the aerial port with a correct output matching network. Note that a correct calculation of the matching network guarantees an optimal power efficiency.

Naturally, the greater the PA output voltage swing, the better the power efficiency. As the PA output is supplied through an inductor, a swing of 2 x V_{DD} is possible. In practice, due to saturation effects, the voltage swing is limited to approximately (2 x V_{DD}) - 1V. With a power supply voltage of 3V, the PA output voltage is 5V peak-to-peak, or 1.77 V_{EFF}.

Figure 24. Output of the Power Amplifier
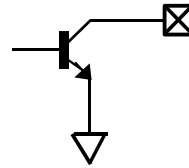
The PA must be correctly matched to deliver the best efficiency in terms of output power and current consumption. Here is an example of the typical recommended output network in the 868 MHz band:

Figure 25. Output Matching at 868 MHz
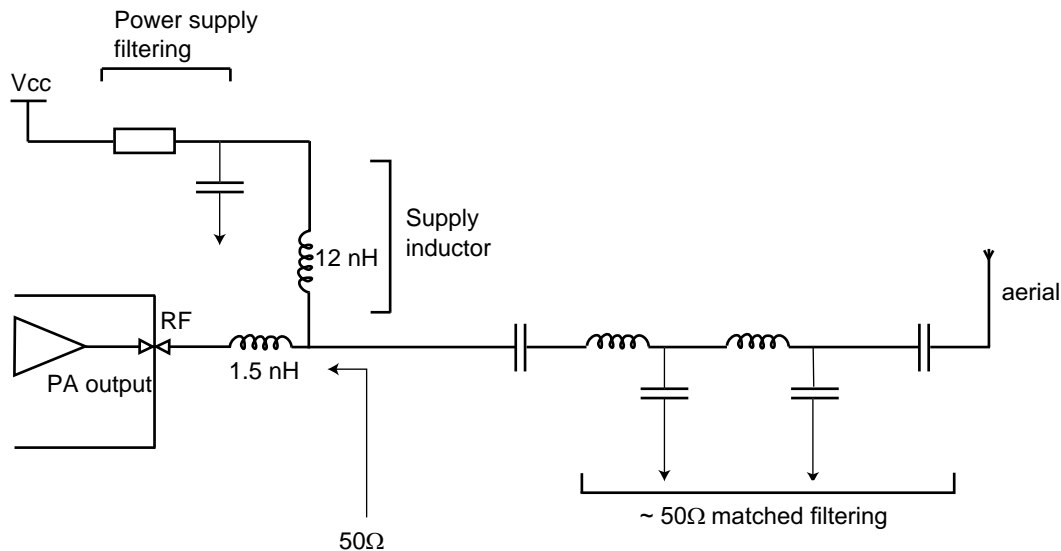
Note: The filter is designed to meet relevant regulations. Please refer to application note for details.

A benefit of this network is to filter the output signal harmonic levels; hence it can be designed to meet a particular regulation.

It is mandatory to implement low impedance grounding techniques. Excessive inductor values to ground will not only limit the PA output voltage swing, but may also trigger RF instability. Board design is vital to avoid parasitic loss when high output power is needed (direct short connection to a single low impedance ground plane).

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An automatic level control loop (ALC) is integrated, in order to minimize the sensitivity of the PA to the temperature, process and power supply variations. For instance, at +85°C, the output power is about 2 dB less than at 25°C. At -40°C, the output power is higher than at 25°C. The ALC is controlled by a current which is generated in the following way:

Figure 26. ALC of the Power Amplifier
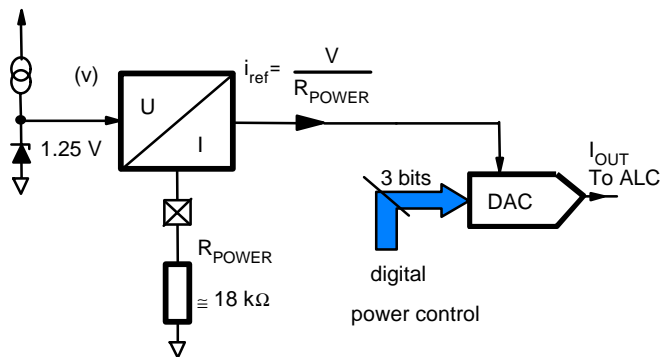
Figure 27. Typical Output Power of the PA for T = 25°C and V_{CC} = 3V
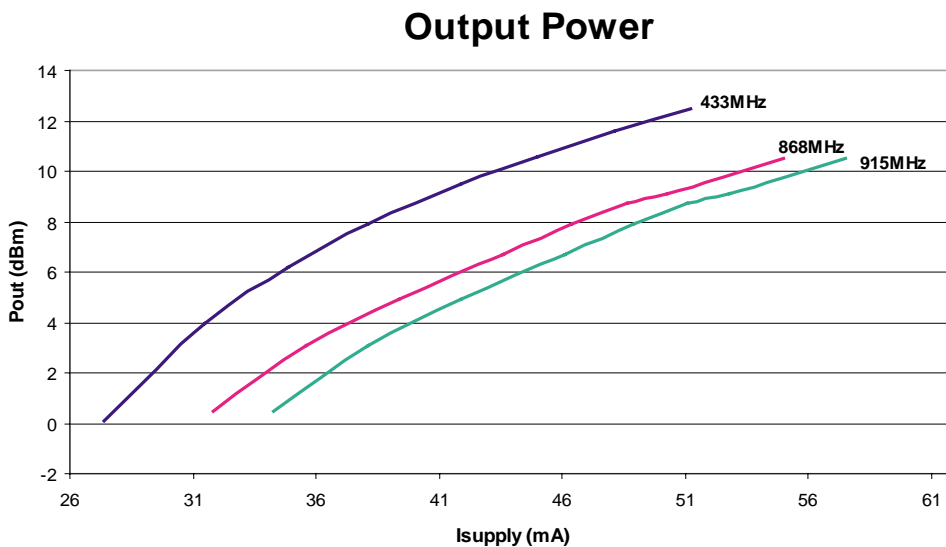
Hardware Control

The max output power is determined by R_{POWER} and the maximum output power is obtained with R_{POWER} = 10 kΩ.

18 kΩ is the nominal value for a +10 dBm output in the 868 MHz frequency band. Decreasing this value to 10 kΩ will lead to +14 dBm at 433 MHz, +12 dBm at 868 MHz, +10 dBm at 915 MHz (typical values for conducted output power).

Figure 28. R_{POWER} Input Schematic
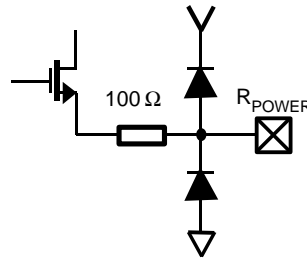
Note: Keeping the PA output matched guarantees maximum power efficiency.

Software Control

The power can then be adjusted, from the value set by R_{POWER} down to a maximum of 12 dB below, by programming the bits 6 to 8 of the CTRL1 register. So, 8 levels are digitally selectable with a variation of the output power. The minimum regulated output power is set to -10 dBm.

Table 3. Software Control of the Power Level

TXLVL (CTRL1)	Pout at 433 MHz (dBm)	Pout at 868 MHz (dBm)	Pout at 915 MHz (dBm)
000	0	-2	-3
001	4	0	0
010	6	3	2
011	8	5	4
100	10	7	5
101	11	8	7
110	12	9	8
111	13	10	9

Note: Unless otherwise specified, typical data given for R_{POWER} = 18 kΩ, T = 25°C, V_{CC} = 3 V

Control Logic

Serial Data Interface

The application microcontroller can control and monitor the AT86RF211 through a synchronous, bidirectional, serial interface made of 3 wires:

• SLE: enable input
• SCK: clock input
• SDATA: data in/out

When SLE = '1', the interface is inhibited, i.e. the SCK and SDATA (in) values are not propagated into the IC, reducing the power consumption and preventing any risk of parasitic write or read cycle.

A "read" or "write" cycle starts when SLE is set to '0' and stops when SLE is set to '1'. Only one operation can be performed in one access cycle: only one register can be either read or written.

- **Register Interface Format**

A message is made of 3 fields:

- address A[3:0]: 4 bits (MSB first)
- R/W: read/write selection
- data D[31:0]: up to 32 bits (MSB first)

ADDRESS				R/W	DATA up to 32 bits (variable length)		
A[3]	A[2]	A[1]	A[0]	R/W	MSB	D[nbit-1:0]	LSB

Variable register length and partial read or write cycles are supported.

In case of partial read or write cycles, the first data (in or out) is always the MSB of the register.

- **WRITE Mode (R/W = 1)**

The address, R/W and data bits are clocked on the rising edge of SCK.

If the number of data bits is lower than the register capacity, the LSB bits keep their former value allowing safe partial write. If the number of data bits is greater than the register capacity, the extra bits are ignored.

The data is actually written into the register on the rising edge of SLE when the data length is less or equal to the register length.

When trying to write more data than the register length, data field is written on the first extra rising clock edge regarding register length.

Figure 29. Write Chronogram: Complete Write Cycle in a 10 bits Register
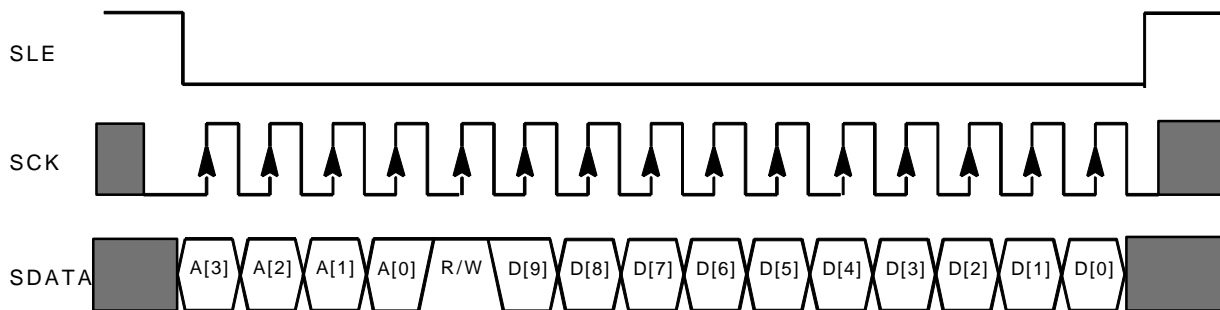
The complete register of 10 bits is updated on a rising edge of SLE.

Figure 30. Write Chronogram: Partial Write Cycle, Writing 2 bits
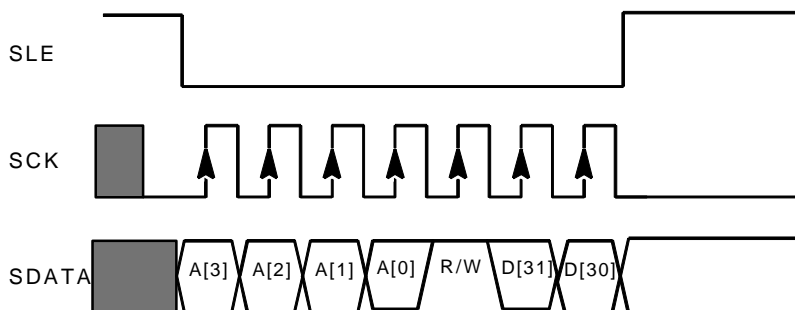
Only the 2 MSBs are updated on the rising edge of SLE; other register bits are unchanged.

- **READ Mode (R/W = 0)**

The address and R/W bits are clocked on the rising edge of SCK.

The data bits are changed on the falling edge of SCK. The MSB of the register is the first bit read.

SDATA I/O pin is switched from input to output on the edge following the "1" clocking the R/W bit.

It is possible to stop reading a register (SLE back to "1") at any time.

If an attempt to read more bits than the register capacity is detected, SDATA is clamped to "0".

If the address of a register is not valid, SDATA is set to "1" during the first 32 SCK periods, then to "0" during all the extra periods.

SDATA is switched back to the input state when SLE is back to "1".

Figure 31. Read Chronogram: Complete Read Cycle from a 10 bits Register
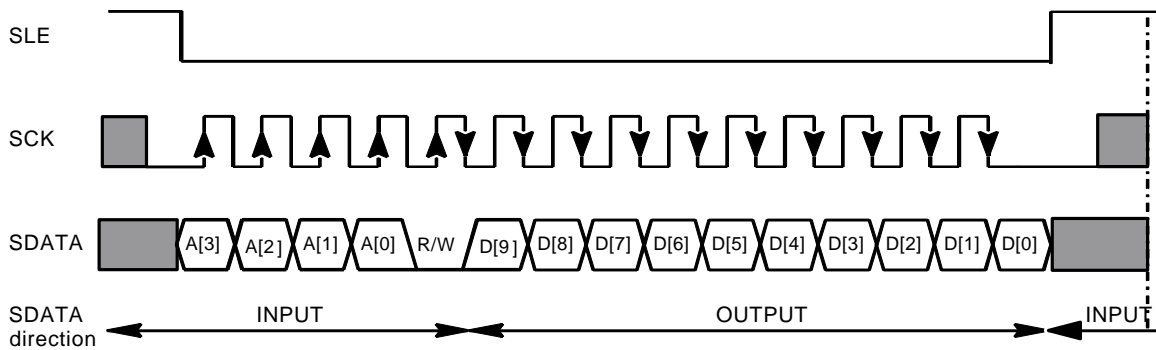
Figure 32. Read chronogram: Partial Read Cycle, Reading 2 bits
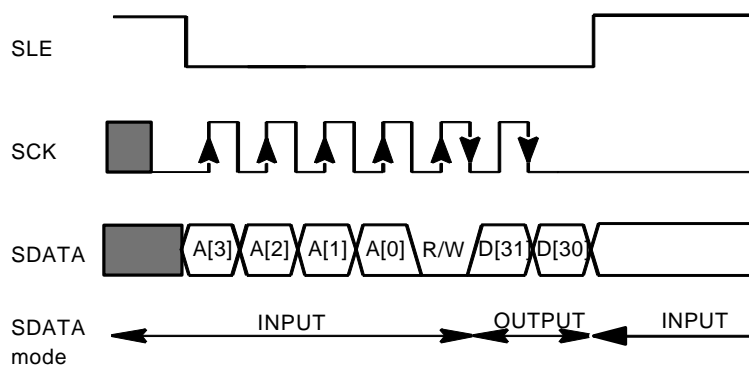
Figure 33. Chronogram with Timing
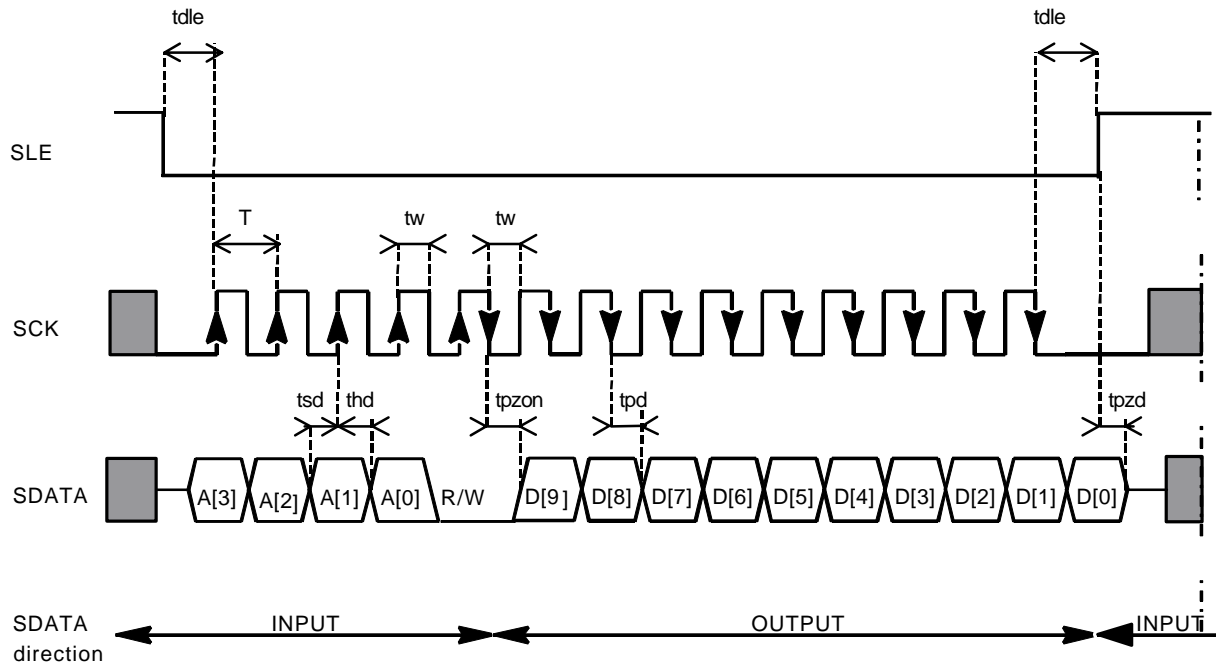
Note: For the timing specification, please refer to the timing table "Digital CMOS DC Characteristics" on page 42.

Registers

Table 4. Registers Overview

Name	Address A[3:0]	Nbits	Read-Write	Comments
F0	$(0000)_2$	32	R-W	F0 Frequency Code
F1	$(0001)_2$	32	R-W	F1 Frequency Code
F2	$(0010)_2$	32	R-W	F2 Frequency Code
F3	$(0011)_2$	32	R-W	F3 Frequency Code
CTRL1	$(0100)_2$	32	R-W	Main Control Register
STAT	$(0101)_2$	31	R	Status Register
DTR	$(0110)_2$	6	R-W	Data Slicer Reference/Discriminator offset adjusting
WUC	$(0111)_2$	32	R-W	Wake-up Control Register
WUR	$(1000)_2$	18	R-W	Wake-up Data Rate Register
WUA	$(1001)_2$	25	R-W	Wake-up Address Register
WUD	$(1010)_2$	32	R	Wake-up Data Register
RESET	$(1011)_2$	1	W	Reset
-	$(1100)_2$			Reserved
-	$(1101)_2$			Reserved
-	$(1110)_2$			Reserved
CTRL2	$(1111)_2$	32	R-W	Control Register (Lock Detect - Clock Recovery)

Note: All the registers must be reprogrammed after the voltage supply has been removed, otherwise they will be in the default state

Reset Register (RESET)

Name	RESET
nbit	0

Writing in this register (0 or 1) triggers an asynchronous reset. This register can only be written.

All registers return to reset state. The chip returns in power-down. So all the following blocks are reset:

- All registers to default value
- Wake-up function.
- Clock recovery function.

And with the power-down state, reset is applied to the following blocks:

- Synthesizer dividers.
- Clock recovery function.
- PLL lock detect.
- From powering up the supplies, it takes about 10 µs or at least 1.8V before the reset state is established (Power-on Reset).
- From reseting the device, one should wait about 10 µs before re-programming
- RSSI detection block.
- Discriminator clock (455 kHz).

Control Register (CTRL1)

Table 5. CTRL1 Overview

Name	PDN	RXTX	DATACLK	TXLOCK	PAPDN	WUEN	LNAGSEL	MVCC	TRSSI	HRSSI
nbit	31	30	29	28	27	26	25	24	23-18	17-15
init	0	0	0	1	0	0	0	0	$(000000)_2$	$(000)_2$

Name	TXLVL	TXFS	-	RXFS	XTALFQ	FSKBW	FSKPOL	DSREF	-	-	MOFFSET	-
nbit	14-12	11	10	9-8	7	6	5	4	3	2	1	0
init	$(000)_2$	0	0	$(10)_2$	0	1	1	1	0	0	0	0

Register reset value = $(10000270)_{16}$

Table 6. CTRL1 Detailed Description[1][2][4][3]

Name	Number of Bits	Comments
PDN	1	General power-down 0: power down mode; only the serial interface is active 1: AT86RF211 activated reset value: 0
RXTX	1	Reception or transmission selection 0: Rx mode 1: Tx mode reset value: 0
DATACLK	1	DATA clock recovery selection 0: no signal on DATACLK output pin 1: Clock recovery active: DATACLK activated reset value: 0
TXLOCK	1	Transmission on PLL lock 0: transmission enabled, regardless of the PLL lock status 1: transmission only when the PLL is locked reset value: 1 note: the PLL status is stored in the PLLL bit of the STATUS register
PAPDN	1	Power amplifier power down 0: Tx Power Amplifier power down mode 1: Tx Power Amplifier activated (only if PDN = 1) reset value: 0
WUEN	1	Wake-up function enable 0: Wake-up function disabled, whatever the content of the wake-up control registers 1: Wake-up function activated, depending on the content of wake-up control registers reset value: 0
LNAGSEL	1	LNA gain selection 0: maximum gain 1: minimum gain reset value: 0
MVCC	1	RSSI or V_{cc} power supply measurement selection 0: RSSI voltage measurement, value is stored in STAT register: MRSSI bits 1: V_{cc} voltage measurement, value is stored in STAT register: MVCC bits reset value: 0
TRSSI	6	RSSI value threshold DATAMSG validated if RSSI $\geq$ TRSSI + HRSSI (high RSSI level) DATAMSG inhibited if RSSI < TRSSI - HRSSI (low RSSI level) reset value: $(000000)_2$
HRSSI	3	Value RSSI hysteresis reset value: $(000)_2$
TXLVL	3	Tx PA output power selection $(000)_2$: minimum transmission level $(111)_2$: maximum transmission level reset value: $(000)_2$
TXFS	1	Tx frequency selection 0: F0 & F1 1: F2 & F3 reset value: 0

Table 6. CTRL1 Detailed Description[(1)(2)(4)(3)] (Continued)

Name	Number of Bits	Comments
–	1	reserved, must be kept to reset value: 0
RXFS	2	RX frequency selection $(00)_2$: F0 $(10)_2$: F2 $(01)_2$: F1 $(11)_2$: F3 reset value: $(10)_2$
XTALFQ	1	Crystal frequency 0: 10.245 MHz (when IF1 = 10.7 MHz) 1: 20.945 MHz (when IF1 = 21.4 MHz) reset value: 0
FSKBW	1	Discriminator range 0: Narrow Discriminator BW 1: Standard Discriminator BW reset value: 1
FSKPOL	1	Polarity of DATAMSG 0: inverted signal 1: direct signal reset value: 1
DSREF	1	Data Slicer reference voltage 0: external reference: SKFILT pin voltage 1: internal reference: DAC level voltage reset value: 1
–	1	reserved, must be kept to reset value: 0
–	1	reserved, must be kept to reset value: 0
MOFFSET	1	0: internal ADC sets to V_{CC} measurement 1: internal ADC sets to DISCOUT DC level measurement reset value: 0
–	1	reserved, must be kept to reset value: 0

Notes: 1. The same ADC is used to measure RSSI or V_{CC} voltage. When the V_{CC} voltage is measured, the RSSI measurement is stopped (previously measured RSSI is kept into STATUS Register). This can disturb the reception process (if a threshold is used for DATAMSG validation). So, it is not recommended to measure V_{CC} in reception mode.
2. V_{CC} measurement can not be done when the AT86RF211 is in power-down mode.
3. While in V_{CC} measurement, it is possible to measure the DC output of the discriminator.
4. Description of RSSI measurement with hysteresis mechanism: if the RSSI measurement is higher than the high RSSI level, DATAMSG is validated (high RSSI level = TRSSI + HRSSI). If the RSSI measure is lower than the low RSSI level, DATA-MSG is inhibited (low RSSI level = TRSSI - HRSSI). Between these two levels, DATAMSG validation depends on the previous measurement.
Example:
TRSSI = 32 and HRSSI = 4 implies High RSSI level = 26 and Low RSSI level = 28

MRSSI sequence	27	32	35	36	35	32	29	28	27	25
RSSI level	NOK	NOK	NOK	OK	OK	OK	OK	OK	NOK	NOK
DATAMSG				valid	valid	valid	valid	valid		

Control Register (CTRL2)
Table 7. CTRL2 Overview

Name	DATARATE	DATATOL	LDCK	N0LD1	N1LD2
nbit	31-18	17-10	9	8-5	4-0
init	$(0000)_{16}$	$(00)_{16}$	0	$(0010)_2$	$(10111)_2$

Register reset value = $(00000057)_{16}$

Table 8. CTRL2 Detailed Description

Name	Number of bits	Comments
DATARATE	14	Received DATAMSG rate This value must be programmed to have the DATACLK activated. (selected with DATACLK bit in CTRL1 register). Value from 1 kbps to 50 kbps reset value: $(0000)_{16}$
DATATOL	8	Tolerance for DATACLK, clock recovery Recommended value = 2% of the rate. reset value: $(00)_{16}$
LDCK	1	Clock frequency is doubled to increase precision of PLL lock detection 0: 10 MHz clock frequency 1: doubled clock frequency reset value: 0
N0LD2	4	PLL unlock condition trigger Recommended values are reset values reset value: $(0010)_2$
N1LD2	5	PLL lock condition trigger Recommended values are reset values reset value: $(10111)_2$

- **Clock Recovery Function**

The clock recovery function is activated by setting to '1' the DATACLK bit of the CTRL1 register.

The clock recovery function provides on DATACLK pin the data clock, synchronized on the received data flow. The targeted position for the rising edge of the clock is the middle of the data bit. It is then easy for the microcontroller to read without synchro troubles.

Clock recovery mechanism is based on the generation of a basic data clock with a period given by DATARATE of CTRL2 with a step of about 100 ns. This basic clock is synchronized on the received data flow with a phase correction step fixed by DATATOL of CTRL2 register (step of about 100 ns also).

So, DATATOL can

- compensate for the difference between the read data rates from transmitter and receiver (fixed by DATARATE).
- allow fast initial synchronization of data clock, avoiding bit transition times and converge toward the middle of the bit.
- keep the right data rate (no additional and no removed bit) when a noisy data with bad bit transition position arrives.

The best value of DATATOL is a trade-off between these considerations. The typical recommended value of RATETOL is 2% of DATARATE.

If the tolerance is too high, the rate value is reached earlier, and the rate value could be unstable (too big step).

If the tolerance is too low, it could be difficult to catch up the DATA and the function could get lost.

Notice that maximum acceptable distance between two data transitions depends on the precision of DATARATE versus transmitter actual data rate.

Synchronization mechanism is explained with the chronogram hereafter. The synchronization is done for the first bit. In worst case conditions, when data and clock arrive at the same time, it begins at the second bit. Notice that the DATACLK signal is available as soon as the DATACLK bit is programmed, whatever the state of DATAMSG pin.

The programmed data rate allows the creation of a basic clock at the programmed DATARATE frequency at the beginning of the reception. Then, the clock is shifted if necessary from the tolerance value, depending on the previous DATA transition: the clock is moved later or sooner, depending on the gap between CLOCK and DATA.

For example:

if DATARATE = 50 kbps, which is equivalent to a duration of 200 x T for 1 bit, with T = 100 ns = base clock period.

if DATATOL = 2% x DATARATE = 4 x T.

Figure 34. Clock Recovery
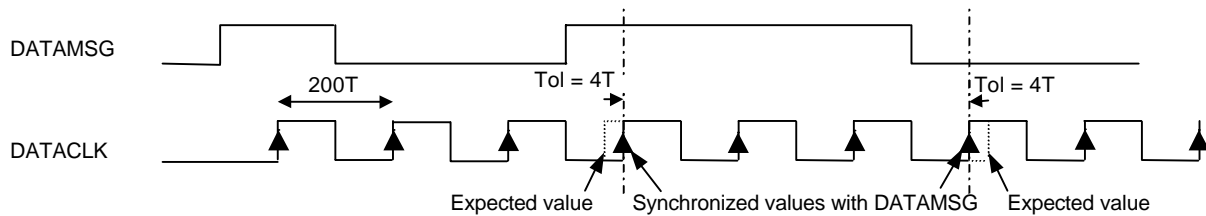
- **DATARATE Programming**

This value must be programmed only when the DATA clock is needed on DATACLK output pin of the chip.

The DATA rate can be programmed from 1 kbps to 64 kbps with 14 bits of CTRL2 register.

DATARATE is the period of the data rate and can be programmed with a resolution given by the crystal oscillator period:

- 10.245 MHz oscillator, period = T = 97.6 ns
- 20.945 MHz oscillator, period = T = 95.5 ns

Some datarate values with the 10.245 MHz oscillator given for example:

DATARATE[13:0]	Rate	Period
$(160)_{10}$	64 kbps	1 bit ~ 160 x T
$(205)_{10}$	50 kbps	1 bit ~ 205 x T
$(vv)_{10}$	……	1 bit ~ vv x T
$(534)_{10}$	19.2 kbps	1 bit ~ 534 x T
$(1024)_{10}$	10 kbps	1 bit ~ 1024 x T

DATARATE[13:0]	Rate	Period
$(1067)_{10}$	9.6 kbps	1 bit ~ 1067 x T
$(2135)_{10}$	4.8 kbps	1 bit ~ 2135 x T
$(4269)_{10}$	2.4 kbps	1 bit ~ 4269 x T
$(10246)_{10}$	1 kbps	1 bit ~ 10246 x T

- **Datatol Programming**

The tolerance for the extraction of DATA rate must be nearly 2% of the RATE. The tolerance represents the step for the calculation of the rate.

If the tolerance is too high, rate value is reached earlier but the rate value could be unstable (step too big).

If the tolerance is too low, it could be difficult to catch up the DATA and the clock recovery could get lost.

Some tolerance values given for example, with tolerance = 2% x DATARATE:

DATATOL[7:0]	Rate	Period
$(3)_{10}$	64 kbps	1 bit ~ 3 x T
$(4)_{10}$	50 kbps	1 bit ~ 4 x T
$(vv)_{10}$	……	1 bit ~ vv x T
$(20)_{10}$	10 kbps	1 bit ~ 20 x T
$(21)_{10}$	9.6 kbps	1 bit ~ 21 x T
$(43)_{10}$	4.8 kbps	1 bit ~ 43 x T
$(85)_{10}$	2.4 kbps	1 bit ~ 85 x T
$(205)_{10}$	1 kbps	1 bit ~ 205 x T

- **PLL Lock Detect**

The PLL lock function uses UP and DOWN signals from the internal phase detector. These signals are analyzed synchronously with a clock frequency, depending of LDCK bit programming (10 MHz or 20 MHz sampling).

LDCK is set to '1' to double the clock frequency of the function PLL lock detect, to increase the precision of the function.

N0LD2 triggers the unlock condition of the PLL.

N0LD2 = number of consecutive edges of the sampling clock with UP and DOWN active before considering PLL unlocked.

This value must not be set to 0 or 1. The recommended value is default value, i.e. 2.

N1LD2 triggers the lock condition of the PLL.

N1LD2 = number of cycle at the PLL reference frequency, without any unlock condition before considering PLL locked.

This value must not be set to 0.

It is recommended to use default values indicated in the table.

Table 9. Frequency Registers

Name	F0, F1, F2, F3
nbit	31-0

Name	Number of bits	Comments
F0	32	Frequency code value F0 default register in TX mode ("0" code in FSK modulation).
F1	32	Frequency code value F1 default register in TX mode ("1" code frequency in FSK modulation).
F2	32	Frequency code value F2 default register in RX mode.
F3	32	Frequency code value F3

Note: 1. F0, F1, F2 and F3 registers must be programmed before using the device.

There is no simple relationship between frequency registers and the exact frequency. Atmel provides a tool to program them on a production bench.

• **Frequency Registers Selection**

The FSK modulation is completely integrated. Two registers have to be programmed (default F0 and F1) to allow "0" and "1" transmission.

The frequency register selection depends on the control register programming and on the DATAMSG pin:

RXTX	RXFS	TXFS	DATAMSG	Mode
0	00	X	X	Receive LO is F0
0	01	X	X	Receive LO is F1
0	10	X	X	Receive LO is F2
0	11	X	X	Receive LO is F3
1	XX	0	0	Transmit "0" on F0
1	XX	0	1	Transmit "1" on F1
1	XX	1	0	Transmit "0" on F2
1	XX	1	1	Transmit "1" on F3

In reception mode, only one frequency needs to be programmed. In transmission mode, two different registers (F0 & F1), or (F2 & F3) must be programmed for "0" code and "1" code transmission. The DATAMSG pin value actually selects the used register. The four registers can also be set to define two channels, so that the AT86RF211 may switch quickly from a channel to the other.

Mode	Programmed Frequency
RX	FCHANNEL ± IF1
TX	FCHANNEL ± deviation

Example:

FCHANNEL = 868.3 MHz
IF1 = 10.7 MHz
Deviation = ± 4 kHz

Mode	FSK
RX	868.3 ± 10.7 = 879 MHz or 857.6 MHz programmed in F2
TX	868.3 ± 0.004 = 868.304 MHz programmed in F1 when DATAMSG = "1" and 868.296 MHz programmed in F0 when DATAMSG = "0"

Notes: 1. In reception mode, one of the two frequencies (879 MHz or 857.6 MHz) can be chosen, taking into account external parameters (for example, the noise that brings the image frequency).
2. Two frequencies are used to transmit data: 868.304 MHz for "1" transmission and 868.296 MHz for "0" transmission. The polarity of DATAMSG can be swapped using bit 5 of CTRL1.

Status Register The STATUS register is used to read the status of internal functions (including the wake-up function) or the output value of the internal ADC. This register can only be read.

Table 10. Status Register Overview

Name	PLLL	MRSSI	MVCC	WAKEUP	-	MSGERR
nbit	30	29-24	23-18	17	16	15

Name	MSGDATL	MSGMRATE
nbit	14-10	9-0

Table 11. Status Register Detailed Description

Name	Number of bits	Comments
PLLL	1	PLL Lock flag 0: PLL unlocked 1: PLL locked reset value: 0
MRSSI	6	Measured RSSI level reset value: $(00)_{16}$
MVCC	6	Measured V_{CC} power supply voltage or discriminator output when MOFFSET = 1 reset value: $(00)_{16}$
WAKEUP	1	WAKEUP flag Copy of the WAKEUP pin, but not affected by polarity selection. 0: no wake-up message received 1: wake-up message received reset value: 0
-	1	Reserved reset value: 0
MSGERR	1	Wake-up message error in test message mode 0: no error detected in the received message 1: message received with error reset value: 0
MSGDATL	5	Wake-up message data length length of the data stored in WUD (received message). reset value: 0
MSGMRATE	10	Wake-up message measured data rate bit period extracted from message header of the wake-up message. Measured as a multiple of 1.56 µs (like RATE in WUR register). 0: 1 x 1.56 µs $(vv)_{10}$: vv x 1.56 µs $(3ff)_{16}$: 1024 x 1.56 µs reset value: $(000)_{16}$

DTR Register   The DTR register allows the user to precisely adjust the offset of the data slicer input.

Table 12. DTR Overview

Name	DSREF[3:0]	DISCHIGH	DISCLOW
nbit	5-2	1	0
init	$(1000)_2$	0	0

Register reset value = $(20)_{16}$

Table 13. DTR Detailed Description

Name	Number of bits	Comments
DSOFFSET	4	Data Slicer reference tuning $(0000)_2$ to $(1111)_2$ reset value: $(1000)_2$
DISCHIGH	1	Discriminator offset shift (high) 0: no shift 1: output level increased reset value: 0
DISCLOW	1	Discriminator offset shift (low) 0: no shift 1: output level decreased reset value: 0

Wake-up Control Register

Table 14. WUC Overview

Name	WUE	DATA	STOP	DATL	ADD	–	WPER	WL1
nbit	31	30	29	28-24	23	22	21-13	12-6
init	0	1	1	$(11111)_2$	1	0	$(001011111)_2$	$(0000100)_2$

Name	WL2	ISTU	–	–
nbit	5-3	2	1	0
init	$(010)_2$	0	0	0

Register reset value = $(7f8be110)_{16}$

Table 15. WUC Detailed Description

Name	Number of bits	Comments
WUE	1	Wake-up function enable Returns to "0" when a valid message is received. 0: wake-up disable 1: wake-up enable reset value: 0
DATA	1	Data content 0: message without data field 1: message with data field reset value: 1
STOP	1	STOP field usage 0: fixed data length: data length set from 1 to 32 by DATL 1: variable data length: data length given by the STOP field location; DATL must be set to $(11111)_2$ reset value: 1

Table 15. WUC Detailed Description (Continued)

Name	Number of bits	Comments
DATL	5	Data length Valid in fixed data length mode (STOP = 0). $(00000)_2$: 1 bit (min data length value) ------------------ $(11110)_2$: 31 bits $(11111)_2$: 32 bits (max data length value) reset value: $(11111)_2$
ADD	1	Address content 0: message without address field 1: message with address field reset value: 1
MSGTST	1	Message error test 0: no error detection mode 1: error detection enabling for debugging reset value: 0
WPER	9	Wake-up period Variable from 10 ms to 328 sec with an accuracy of ±20%.(on-chip RC oscillator) reset value: 960 ms reset value: $(5f)_{16}$
WL1	7	Minimum delay before TEST1 (check of RSSI level) Variable from 1ms to 1.024 sec Delay calculation starts when the reference oscillator starts reset value: 5 ms reset value: $(04)_{16}$
WL2	3	Minimum delay between TEST 1 and TEST 2 (check of header detection) Variable as multiple of WL1 from 0 to 31 x WL1 reset value: 2 x WL1 reset value: $(2)_{10}$
ISTU	1	Inhibit stuff mechanism 0: stuff is used for wake-up message 1: no stuff used in the wake-up message reset value: 0
-	2	Reserved, must be kept to reset value reset value: 0

- **WPER Programming**

WPER can be set from 10 ms to 328 sec with an accuracy of ±20%. A 10 ms period clock is used for this period generation.

Bit 8 and 7 give a period multiplication factor of 1, 16 or 256 (with two serial by 16 clock prescalers).

Bit 6 to 0 give the number of cycles of the divided clock from 1 to 128 (counter).

Table 16. Wake Up Period Programming

WPER[8:0]	WPER[8:7]	WPER[6:0]	Period	Prescaler	Comments
$(000)_{16}$	$(00)_2$	$(00)_{16}$	10 ms	1	1 x 10 ms
$(001)_{16}$	$(00)_2$	$(01)_{16}$	20 ms	1	(1+1) x 10 ms
–	$(00)_{10}$	$(vv)_{10}$	–	1	(vv +1) x 10 ms
$(07e)_{16}$	$(00)_2$	$(7e)_{16}$	1270 ms	1	1 x 1270 ms
$(07f)_{16}$	$(00)_2$	$(7f)_{16}$	1280 ms	1	1 x 1280 ms
$(101)_{16}$ or $(081)_{16}$	$(10)_2$ or $(01)_2$	$(01)_{16}$	170 ms	16	((16 x 1)+1) x 10 ms
$(102)_{16}$ or $(082)_{16}$	$(10)_2$ or $(01)_2$	$(02)_{16}$	330 ms	16	((16 x 2)+1) x 10 ms
–	$(10)_2$ or $(01)_2$	$(vv)_{10}$	–	16	((16 x vv)+1) x 10 ms
$(17e)_{16}$ or $(0fe)_{16}$	$(10)_2$ or $(01)_2$	$(7e)_{16}$	20.2 sec	16	((16 x 126)+1) x 10 ms
$(17f)_{16}$ or $(0ff)_{16}$	$(10)_2$ or $(01)_2$	$(7f)_{16}$	20.3 sec	16	((16 x 127)+1) x 10 ms
$(181)_{16}$	$(11)_2$	$(01)_{16}$	2.57 sec	256	((256 x 1)+1) x 10 ms
$(182)_{16}$	$(11)_2$	$(02)_{16}$	5.13 sec	256	((256 x 2)+1) x10 ms
–	$(11)_2$	$(vv)_{10}$	–	256	((256 x vv) +1) x 10 ms
$(1fe)_{16}$	$(11)_2$	$(7e)_{16}$	323 sec	256	((256 x 126)+1) x 10 ms
$(1ff)_{16}$	$(11)_2$	$(7f)_{16}$	325 sec	256	((256 x 127)+1) x 10 ms

- **WL1 Programming**

WL1 can be set from 1 ms to 1.024 sec. A 1 ms period clock is used for this delay generation.

Bit 6 gives a period multiplication factor of 1 or 16 (by 16 clock prescaler).

Bits 5 to 0 give the number of cycles of the divided clock from 1 to 64 (counter).

Table 17. WL1 Programming

WL1[6:0]	WL1[6]	WL1[5:0]	Period	Prescaler	Comments
$(00)_{16}$	0	$(00)_{16}$	1 ms	1	1 x 1 ms
$(01)_{16}$	0	$(01)_{16}$	2 ms	1	(1+1) x 1 ms
$(vv)_{10}$	0	$(vv)_{10}$	vv + 1 ms	1	1x (vv +1) ms
$(3e)_{16}$	0	$(3e)_{16}$	63 ms	1	1 x 63 ms
$(3f)_{16}$	0	$(3f)_{16}$	64 ms	1	1 x 64 ms
$(40)_{16}$	1	$(00)_{16}$	16 ms	16	16 x 1 ms
$(41)_{16}$	1	$(01)_{16}$	32 ms	16	16 x 2 ms
–	1	$(vv)_{10}$	–	16	16 x (vv +1) ms
$(7e)_{16}$	1	$(3e)_{16}$	1.008 sec	16	16 x 63 ms
$(7f)_{16}$	1	$(3f)_{16}$	1.024 sec	16	16 x 64 ms

- **WL2 programming**

WL2 can be set as a multiple of WL1 from 0 to 31 WL1.

Table 18. WL2 Programming

WL2[2:0]	Period	Comments
$(000)_2$	0	Simultaneous test of the RSSI and the header
$(001)_2$	1 x WL1	
$(010)_2$	2 x WL1	
$(011)_2$	3 x WL1	
$(100)_2$	4 x WL1	
$(101)_2$	8 x WL1	
$(110)_2$	16 x WL1	
$(111)_2$	31 x WL1	

Wake-up Data Rate Register
(WUR)

Table 19. WUR Overview

Name	WUOP	RATECHK	RATE	RATETOL
nbit	17-16	15	14-5	4-0
init	$(01)_2$	0	$(0000010000)_2$	$(01000)_2$

Table 20. WUR Detailed Description

Name	Number of bits	Comments
WUOP	2	WAKEUP output polarity $(00)_2$: WAKEUP pin active low $(01)_2$: WAKEUP pin active high $(1x)_2$: WAKEUP pin open drain (active low, inactive tri-state) reset value: $(01)_2$
RATECHK	1	Data rate check the data rate is automatically extracted from the HEADER field. the data rate can be compared to RATE with a tolerance of plus or minus RATETOL. Data rate is computed from a unit of 1.56 µs (Reference clock divided by 16). 0: data rate not checked. 1: data rate check done (header ignored if check fails). reset value: 0
RATE	10	Data rate value 0d: min value = 1 x 1.56 µs $(1023)_{10}$: max value = 1024 x 1.56 µs reset value: 64 x 1.56 µs reset value: $(63)_{10}$
RATETOL	5	Data rate tolerance 0d: min value = 0 x 1.56 µs $(31)_{10}$: max value = 31 x 1.56 µs reset value: 8 x 1.56 µs reset value: $(8)_{10}$

The data rate (in bps) and the decimal value to be coded in the register are related by the equation:

$$RATE = \frac{640000}{rate\ (bps)}$$

The following table gives the programming values of commonly used rates:

Rate	WUR RATE
1200 bits/sec	$(533)_{10}$
2400 bits/sec	$(267)_{10}$
4800 bits/sec	$(133)_{10}$
9600 bits/sec	$(67)_{10}$

Wake Up Address Register (WUA)

Table 21. WUA Overview

Name	ADDL	ADD
nbit	24-20	19-0
init	$(01001)_2$	$(0f0f0)_{16}$

Table 22. WUA Detailed Description

Name	Number of bits	Comments
ADDL	5	Wake-up address length 0: wake-up address length = 1 bit 1: wake-up address length = 2 bits .... $(19)_{10}$: wake-up address length = 20 bits $>(19)_{10}$: forbidden reset value: 10 bits
ADD	20	Wake-up address If wake-up address length is less than 20 bits, MSB bits are ignored reset value: $(0f0f0)_{16}$

Concerning this register, attention should be paid to the fact that the last bit of the address field is not taken into account when testing the address field that is received. Thus the last bit must be programmed and counted in the address length but it can be either "0" or "1".

Wake-up Data Register (WUD)

Table 23. WUD Overview

Name	WUD
nbit	(data length -1) - 0

Table 24. WUD Detailed Description

Name	Number of bits	Comments
WUD	Length	Wake-up message data Warning: The length of this register is variable: * case fixed data length (STOP = 0 of WUC) data length is given by DATL of WUC. * case variable data length (STOP = 1 of WUC) data length is given by MSGDATL of STAT register. Warning: The first bit of received data is the LSB: WUD[0].

Note: To use this mode, please refer to the corresponding application note.

Electrical Specification

ESD sensitive device: storage or handling of the device must be carried out according to usual protection rules.

Absolute Maximum Ratings

Temperature	+95°C
Storage temperature	-65 to +150°C
Supply voltage	0 to 3.95V
Digital input voltage	-0.3 to V_{CC} + 0.3V
RXIN input power	0 dBm

Note: Stresses beyond the conditions listed above may cause permanent damage to the device. Exposure to Absolute Maximum Ratings conditions for an extended period may affect device reliability.

DC Characteristics

Unless otherwise specified, data is given for T = 25°C, V_{SUPPLY} = 2.7V

Parameter	Min	Typ	Max	Unit	Comment
Supply voltage	2.4		3.75	V	[1]
Supply current		0.5		μA	Power-down
Supply current		3		μA	Sleep mode
Supply current		29		mA	Rx mode
Supply current		35		mA	Tx mode, Pout = +10 dBm at 433 MHz
Supply current		20		mA	Tx mode, PDN-PA on
Operating temperature	-40		+85	°C	

Note: 1. The allowed supply voltage of the AT86RF211 is higher than 3.75V. However, we strongly recommend not to exceed 3.75V from now on, to be compliant with future versions of the device.

Digital CMOS DC Characteristics

Unless otherwise specified, data is given for T = 25°C, V_{SUPPLY} = 2.7V

Name	Parameter	Conditions	Min	Typ	Max	Units
Vil	CMOS low level input voltage - Normal input[2] - Schmitt trigger input[3]				0.3*Vcc 0.2*Vcc	V V
Vih	CMOS high level input voltage - Normal input[2] - Schmitt trigger input[3]		0.7*Vcc 0.85*Vcc			V V
Vol	CMOS low level output voltage[1]	Iol = 1 mA			0.2*Vcc	V
Voh	CMOS high level output voltage[1]	Ioh = - 1 mA	0.8*Vcc			V

Note: 1. For digital CMOS pins : SDATA, DATAMSG, DATACLK, WAKEUP.

2. For digital CMOS pins: SLE, SCK, SDATA
3. For digital CMOS pins: DATAMSG

• **Timings**

Name	Parameter	Conditions	Min	Typ	Max	Units
tr = tf	CMOS rise/fall times	C_L = 50 pF ; 20% to 80%			30	ns
F	SCK frequency		0		5	MHz
T	SCK period		200			ns
tw	SCK low or high time		60			ns
tsd	SDATA setup before SCK rising		40			ns
thd	SDATA hold after SCK rising		40			ns
tpd	SDATA output propagation delay after SCK falling (read mode) (C_L = 30 pF)		2		50	ns
tpzon	Delay to switch SDATA to output after SCK falling (read mode)		3		50	ns
tdle	Minimum delay between an edge of SLE and an edge of SCK		40			ns
tpzd	Delay to switch SDATA to input (tri-state) after SLE rising (read mode)				40	ns
C_L[1]	Max load for CMOS output pins				50	pF

Note: These timings refer to the Figure 33 on page 25.

Synthesizer Specification

Unless otherwise specified, data is given for T = 25°C, V_{SUPPLY} = 2.7V

Parameter	Min	Typ	Max	Unit	Comments
Frequency Range	400		480	MHz	Digital programming
Frequency Range	800		950	MHz	Digital programming
Crystal Frequency	10.235	10.245	10.255	MHz	IF 1 = 10.7 MHz[1]
Crystal Frequency	20.925	20.945	20.965	MHz	IF 1 = 21.4 MHz[1]
Oscillator Settling Time	5	8		ms	Depending on crystal specifications
Lock Time[2]		300		µs	From oscillator settling
Lock Time[2]		30		µs	100 kHz shift
Phase Noise 400 to 480 MHz		-80		dBc/Hz	At 10 kHz from the carrier
Phase Noise 800 to 950 MHz		-75		dBc/Hz	At 10 kHz from the carrier
Phase Noise 400 to 480 MHz		-91		dBc/Hz	At 100 kHz from the carrier
Phase Noise 800 to 950 MHz		-86		dBc/Hz	At 100 kHz from the carrier

Notes: 1. Crystal frequency can be slightly changed but since IF2 = IF1 - Crystal frequency, IF2 will shift and must remain within the IF2 filter and discriminator bandwidth.
2. With the "typical implementation" loop filter.

Receiver Specification

Unless otherwise specified, data is given for T = 25°C V_{SUPPLY} = 2.7V

Parameter	Min	Typ	Max	Unit	Comments
IF1		10.7		MHz	21.4 MHz also possible
IF1 Filter Impedance		330		Ω	
IF2		455		kHz	
IF2 Filter Impedance		1700		Ω	
FSK Sensitivity		-105		dBm	Typical performance with a BER of 1% at input pin RXIN (45). BW = ± 10 kHz, ΔF = ± 7.5 kHz; Brate = 4800 bps[1]
Noise Figure		15		dB	Input matched, complete RX chain
Input IP3		-15		dBm	
Max Input Power			-5	dBm	BER < 10%

Note: 1. The overall sensitivity depends on measurements conditions and external components, i.e.:
-100 dBm for BW = ± 10 kHz, ΔF = ± 7.5 kHz, Brate = 4800 bps with RF switch used and external SAW filter

Transmitter Specification

Unless otherwise specified, data is given for T = 25°C, V_{SUPPLY} = 2.7V, R_{POWER} = 18 kΩ.

Parameter	Min	Typ	Max	Unit	Comments
Output Power	+10	+14		dBm	433 MHz band[1]
Output Power	+10	+12		dBm	868 MHz band[1]
Output Power	+8	+10		dBm	915 MHz band[1]
Output Power Dynamic Range		12		dB	Digital programming[2]
Automatic Level Control Accuracy		1		dB	Constant conditions
Automatic Level Control Accuracy		± 2		dB	Against V_{CC}, T°[3]
FSK Data Rate			64	kbps	
RX to TX Toggle Time		200		µs	Typical loop filter implementation

Notes: 1. Output power for R_{power} = 10 kΩ and TXLVL = "111"

2. The maximum power is set by an external resistor, connected to pin R_{POWER}. The output power can be digitally programmed/re-programmed, up to -12 dB below this limit, by means of a 3-bit word: TXLVL of CTRL1 register.

3. The output power is regulated against process, temperature and power supply variations by an internal ALC loop.

Typical Application

Implementation
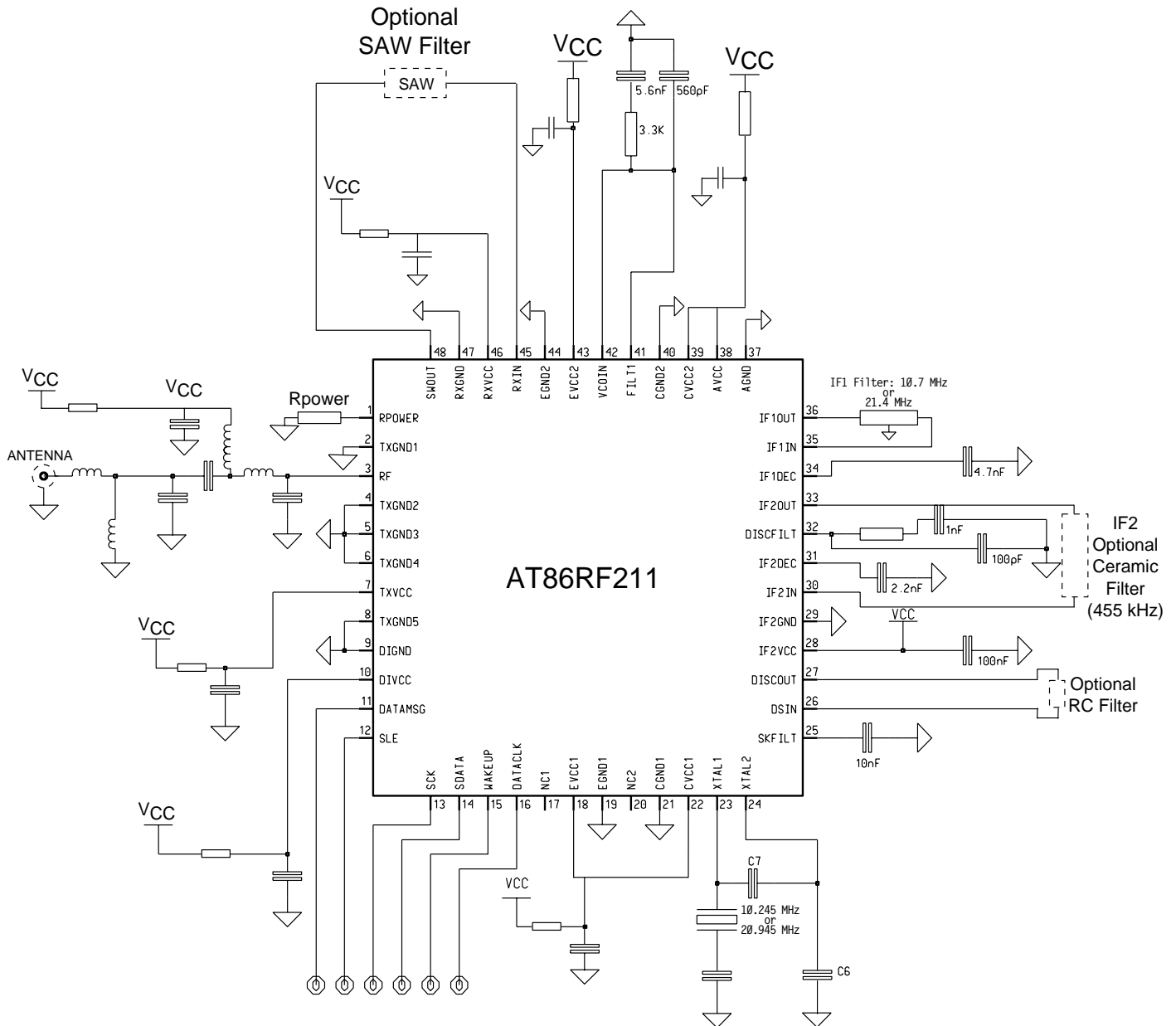
Note: Accurate information about parts and values of components to be used around AT86RF211 are described in our application notes. "RF Bill-of-Material/cost for 868-915 MHz applications".

Layout

Reference Design Top Layer

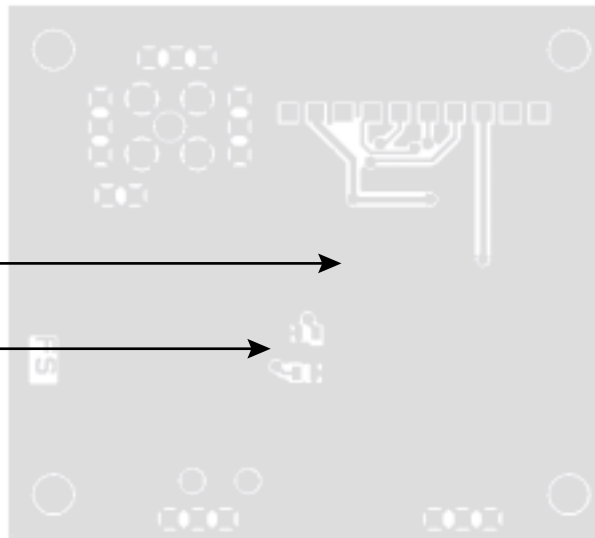Each unused area must be filled with copper and connected to the bottom side ground plane

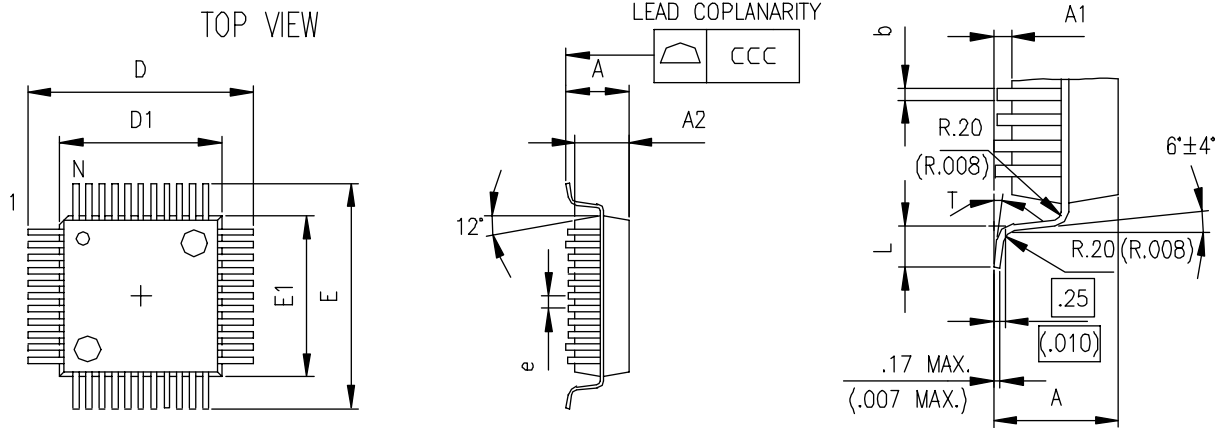Decoupling capacitors remain close to the supply pins
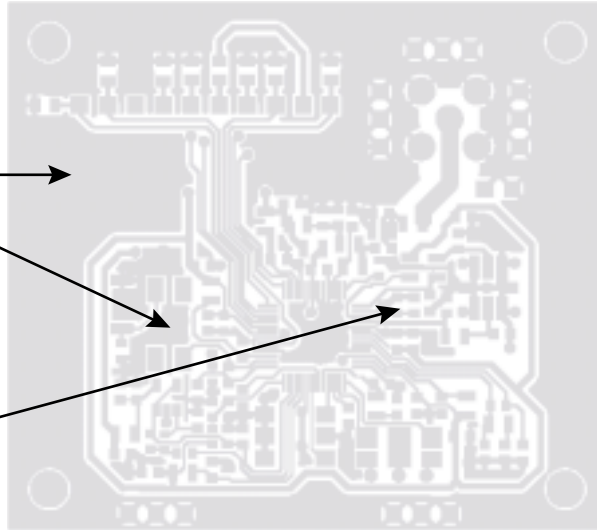
Reference Design Bottom Layer

One-block ground plane with no slot under the whole RF area

This small slot is allowed as it is under the RF211: thus there is no track above

Packaging Information

48 lead TQFP

Dimension	Nominal Value (mm)	Tolerance
A	1.60	max
A1	0.05 min/0.15 max	
A2	1.40	±0.05
D	9.00	±0.20
D1	7.00	±0.10
E	9.00	±0.20
E1	7.00	±0.10
L	0.60	+0.15/-0.10
e	0.50	basic
b	0.22	±0.05
ccc	0.1	max

Dimension	Nominal Value (inch)	Tolerance
A	0.063	max
A1	0.002 min/0.06 max	
A2	0.055	±0.002
D	0.354	±0.008
D1	0.275	±0.004
E	0.354	±0.008
E1	0.275	±0.004
L	0.024	+0.006/-0.004
e	0.020	basic
b	0.009	±0.002
ccc	0.004	max

Ordering information

Full Part Number	Package	Conditionning
AT86RF211 DAI	TQFP48	Tray
AT86RF211 DAI-R	TQFP48	Tape & reel

Atmel Headquarters

Corporate Headquarters
2325 Orchard Parkway
San Jose, CA 95131
TEL 1(408) 441-0311
FAX 1(408) 487-2600

Europe
Atmel Sarl
Route des Arsenaux 41
Case Postale 80
CH-1705 Fribourg
Switzerland
TEL (41) 26-426-5555
FAX (41) 26-426-5500

Asia
Room 1219
Chinachem Golden Plaza
77 Mody Road Tsimhatsui
East Kowloon
Hong Kong
TEL (852) 2721-9778
FAX (852) 2722-1369

Japan
9F, Tonetsu Shinkawa Bldg.
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
Japan
TEL (81) 3-3523-3551
FAX (81) 3-3523-7581

Atmel Operations

Memory
2325 Orchard Parkway
San Jose, CA 95131
TEL 1(408) 441-0311
FAX 1(408) 436-4314

Microcontrollers
2325 Orchard Parkway
San Jose, CA 95131
TEL 1(408) 441-0311
FAX 1(408) 436-4314

La Chantrerie
BP 70602
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FAX (44) 1355-242-743

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Theresienstrasse 2
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74025 Heilbronn, Germany
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FAX 1(719) 540-1759

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High Speed Converters/RF Datacom
Avenue de Rochepleine
BP 123
38521 Saint-Egreve Cedex, France
TEL (33) 4-76-58-30-00
FAX (33) 4-76-58-34-80

e-mail
literature@atmel.com

Web Site
http://www.atmel.com

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