Freescale Semiconductor, Inc.
User's Guide

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EVB-VF522R3 Platform User's Guide

1 Introduction

This user's guide details the setup and configuration of the Freescale Automotive Evaluation Board (hereafter referred to as the EVB). The EVB is intended to provide a mechanism for easy customer evaluation of the heterogeneous dual-core Vybrid family, and to facilitate hardware and software development.

The SVF522R3K1CMK4 MCU used on the EVB has following characteristics:

- 500 MHz 32-bit ARM® Cortex®-A5 core,
- Dual TFT display,
- Dual USB OTG with built-in HS / FS / LS PHY,
- Dual 10 / 100 MAC (Ethernet) with L2 switch,
- Advanced security,
- -40°C to 85°C operating temperature range.

The EVB as a whole, however, is intended for bench / laboratory use and has been designed using commercial temperature-range specified components (up to +70°C).

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CAUTION

The EVB contains components that may be damaged by electrostatic discharge. Observe precautions for handling electrostatic-sensitive devices when using this EVB.

1.1 Peripheral daughtercards

The EVB has connectors / headers for various daughtercards that provide additional peripheral functionality (see Section 14, "User I/O and control" for details). These are not supplied with the EVB and may be sourced separately.

CAUTION

Daughtercards are usually not hot-swappable; ensure that the EVB is powered OFF prior to fitting or removing a daughtercard.

2 Features

Shown in Figure 1, the EVB has the following features:

- Single 12V ± 2V / 2A DC external power supply input (via a 2.1 mm barrel-style power jack) with on-board voltage regulators.
- LED status indication for all the power rails.
- Inherent "Enable" for the major power rails.
- Power-on, manual, and JTAG reset with status LED.
- Configurable reset multiplexer (controlled over SPI/I^2C) providing reset control of the major peripheral blocks.
- RCON (reset configuration) jumpers and full 32-bit switches.
- 20-pin JTAG and 10-pin ARM Cortex debug headers.
- Two incremental encoders and four dedicated station preset buttons.
- High-speed CAN transceiver routed to 4-pin header.
- SCI transceiver (routed to standard DB9 connector) and LIN transceiver (routed to Molex 4-pin connector) on shared SCI0 channel.
- Board-to-board MAC (Ethernet) connector, e.g. for Ethernet daughtercard.
- Two MCU USB interfaces based on "On-The-Go Micro AB" and "Type A Host" connectors with full 500 mA support each.
- 1G (64M x 16) DDR3 SDRAM IC.
- Three QuadSPI Flash ICs, 256 MB each.
- SD card slot.
- Four "Video In" (RCA "phono") inputs with direct connection to MCU video ADC.
- Unified 24-bit DCU connector (QSH-060-01-L-D-A) with analog and I^2C support for basic touch screen operation; matches Freescale LCD and HDMI daughtercards.
- MLB daughtercard connector.

- Potentiometer (variable resistor) on MCU ADC channel 0.
- Headers for all accessible, GPIO and analog, signals not used elsewhere on the EVB.
- “Aux in” audio connector (3.5 mm), with filter and standalone ADC IC.
- Left and right SPI-based microphones.
- Standalone DSP for audio processing.
- SPI Serial Flash IC, 32 MB (dedicated to DSP, optional usage).
- Twin DAC, filter, and headphone amplifiers for audio outputs (3.5 mm connectors).
- Radio tuner daughtercard connector.
- Two I^2C daughtercard connectors.
- Bluetooth® daughtercard connector.
- Generic CD connector.

NOTE

To alleviate confusion between jumpers and headers, all EVB jumpers are implemented as 2 mm pitch, whereas headers are 0.1” (2.54 mm). This prevents inadvertently fitting a jumper to a header.

CAUTION

Before the EVB is used or power is applied, please, fully read this user manual.

Failure to correctly configure the board may cause irreparable damage.

Power must be removed from the EVB prior to:

- Removing or installing daughtercards or other connectors.
- Reconfiguring the board jumpers or switches.

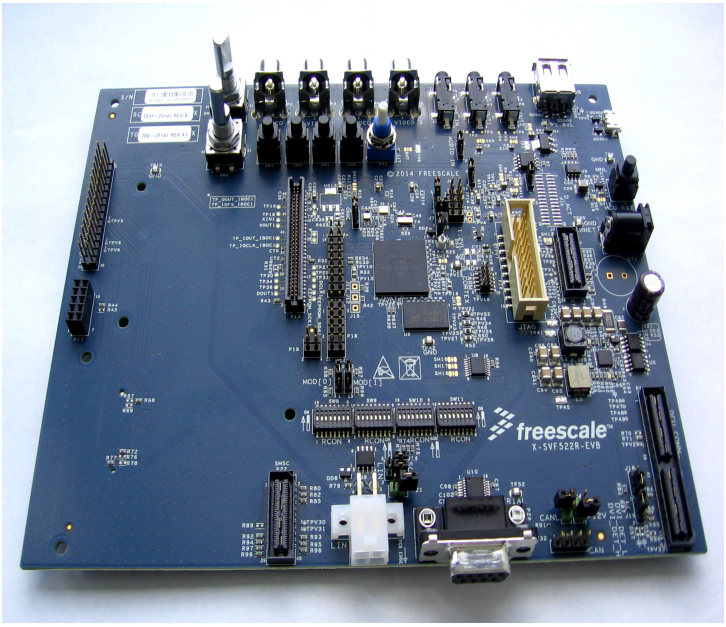

Figure 1. Freescale Automotive Evaluation Board (EVB) overview

3 Configuration overview

The EVB has been designed with ease of use in mind; its functional blocks are shown in Figure 2 and Figure 3 below. Explained are the power, reset, clocks, and debug configuration settings, which are the minimum required to power on the EVB.

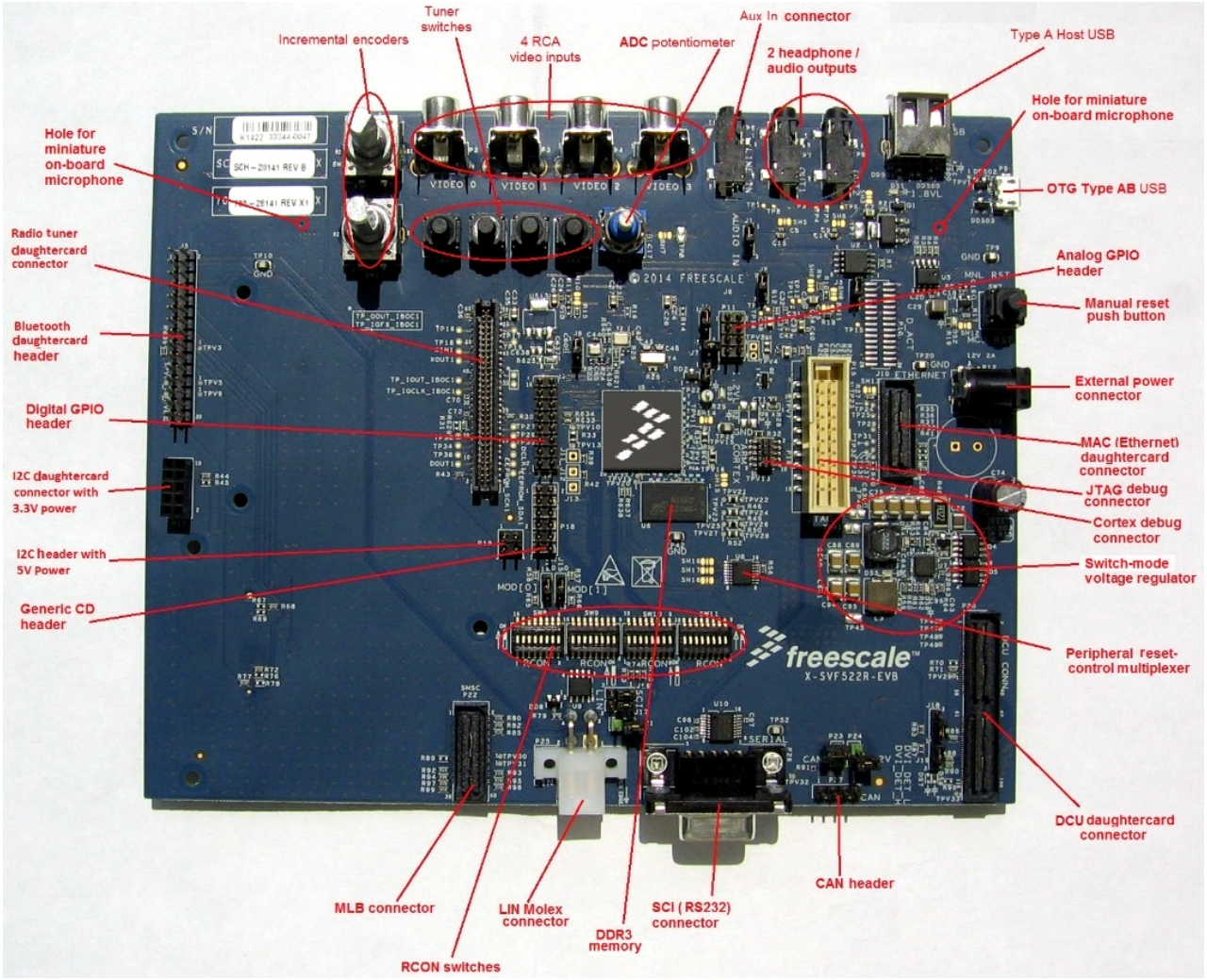

Figure 2. EVB functional blocks (top view)

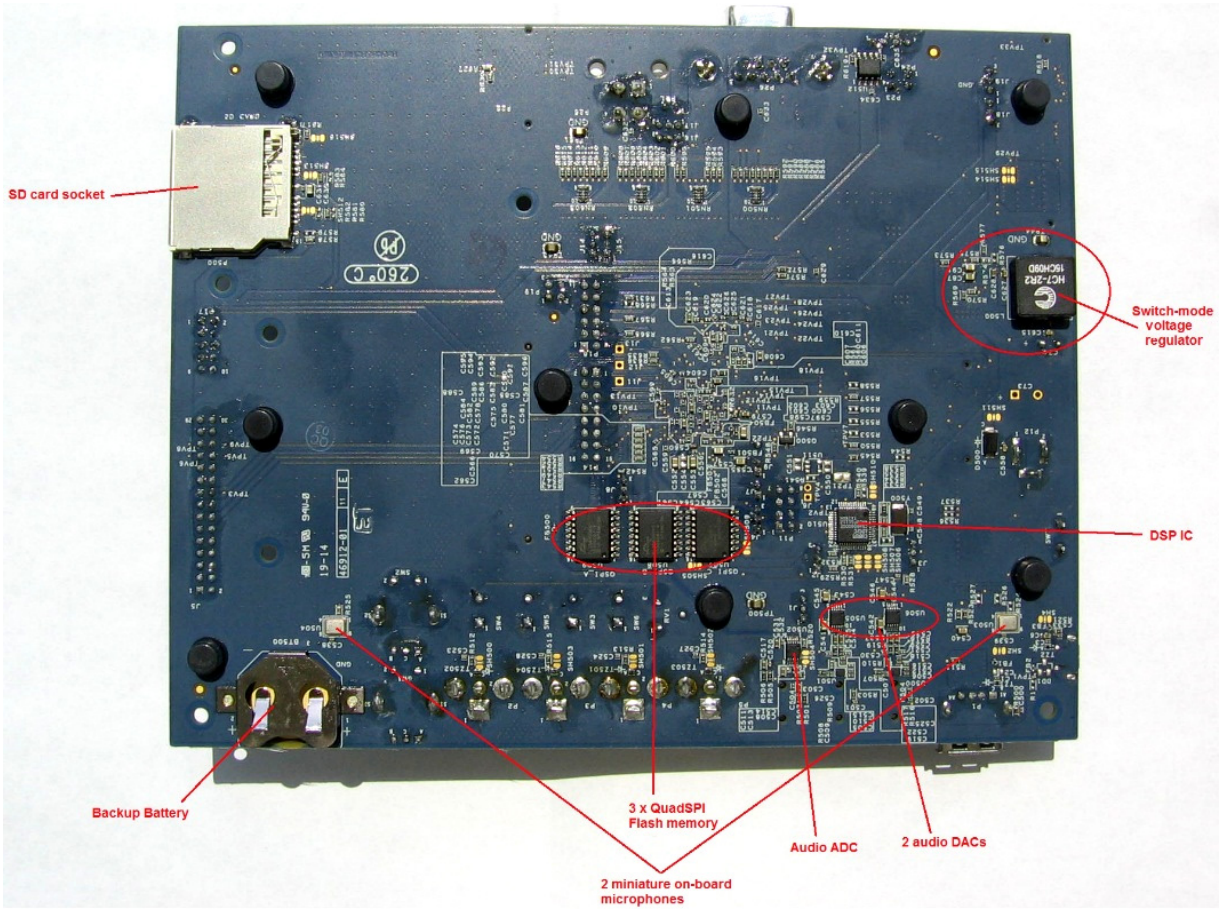

Figure 3. EVB functional blocks (top view)

4 Power management scheme

4.1 External power connector (P12)

The EVB requires a DC supply of 12V ± 2V capable of 2A, which allows easy use in a vehicle as well as copying the design for automotive applications. A standard 2.1 mm barrel connector type is used. Care must be taken to ensure the correct polarization as shown in Figure 4 below.

Figure 4. 2.1 mm power connector

4.2 Switch-mode voltage regulator (U7)

An automotive-grade triple-output switch-mode voltage regulator generates:

- 1.5V to power the main MCU core voltage regulator (default), MCU DDR interface, and DDR memory,
- 3.3V to power the main MCU core voltage regulator (to test low-power applications, e.g. without DDR), main MCU supply, and EVB peripherals,
- 5V to power the MCU USB interface and EVB peripherals.

Each output has a “Power-Good” LED indicator as well as an inherent “Enable” feature.

4.3 Linear voltage regulators (U511, U1, U513)

Three voltages are generated using linear voltage regulators:

- Optional 1.2V to power the MCU analog 1.2V blocks (instead of using filtered MCU core supply),
- 1.8V to power the audio/DSP circuitry,
- Optional 3.3V to power the MCU analog 3.3V blocks and other EVB circuitry (instead of using filtered MCU supply).

The 1.2V and 1.8V outputs have LED status indicators.

4.4 Power status LEDs (DS1 to DS6)

Five voltage outputs have green LED status indicators as shown in Table 1.

Table 1. Power status LEDs

LED	Legend	Description
DS1	1.8VL	Linear 1.8V
DS3	1.2VL	Linear 1.2V
DS4	1.5VS	Switch-mode 1.5V “Power-Good”
DS5	3.3VS	Switch -mode 3.3V “Power-Good”
DS6	5VS	Switch -mode 5.0V “Power-Good”

If no LEDs are illuminated when power is applied to the EVB, it is possible that the external power source polarity is incorrect. The EVB will not be damaged, though, thanks to the series diode D500 on the power input.

Although all the voltage regulators have output overload protection, it is strongly recommended to prevent their outputs from being shorted. If this happens, damage is likely to occur to the EVB and/or components.

4.5 Backup battery (BT500)

When the external power supply fails, the Secure Real-Time Clock (SecureRTC) module of the MCU operates from the on-board coin cell battery. Its holder accommodates a 20 mm diameter 3V lithium-ion

battery, for example 2032 or 2025, and the J8 header (see Table 15) selects if the MCU VBAT pin is powered from it or the main MCU 3.3V rail (see Figure 5).

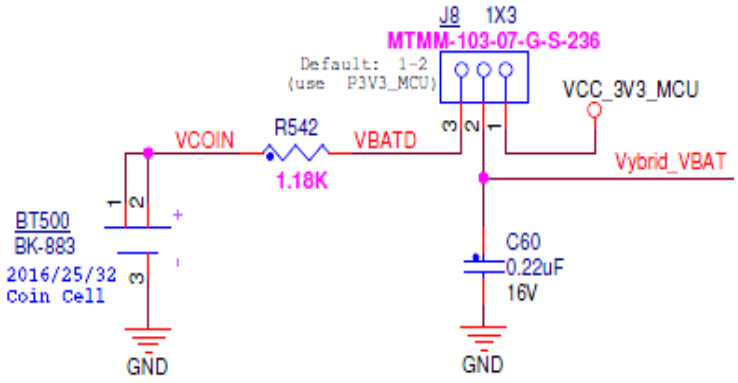

Figure 5. Backup battery

4.6 MCU supply routing

4.6.1 MCU core power

An external ballast transistor (Q2) is used to generate 1.2V for the MCU core (see Figure 6); depending on the R28 configuration (see Table 15), its collector can be powered from one of the below rails:

- 1.5V (default),
- 3.3V (to test low-power applications without 1.5V rail, e.g. without DDR); in this case, the optional diodes D2 and D3 shall be populated.

Refer to the AN4807 Application Note for details.

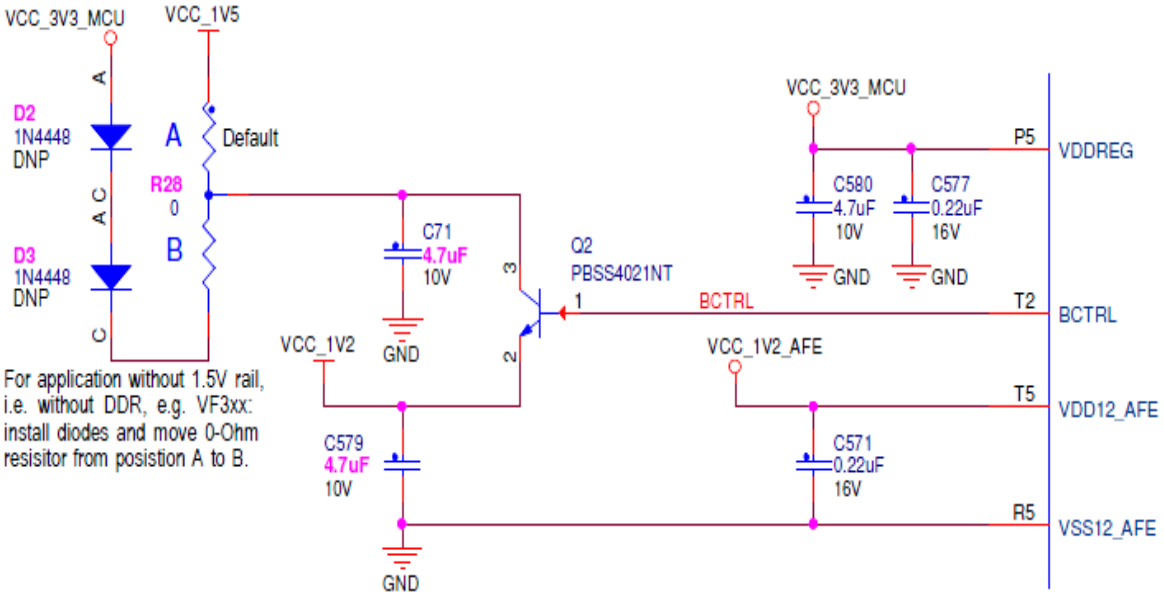

Figure 6. MCU core power

4.6.2 Analog MCU power scheme

The four analog MCU power rails, VDD12_AFE, VCC_3V3_AFE, VCC_3V3_ADC, and VREF_3V3, have two powering options (see Figure 7):

1. The default, cost-efficient option through a series ferrite bead filtering the relevant main power rail,
2. The optional, more expensive option when high-quality ADC and DAC performance required - from the dedicated linear voltage regulators (unpopulated by default).

Details of using the option-selection components, FB504, R632, and R625, as well as J6, the ON/OFF jumper for the optional linear 1.2V regulator (U511), are described in Table 15.

The optional linear 3.3V regulator (U513) does not have an ON/OFF feature

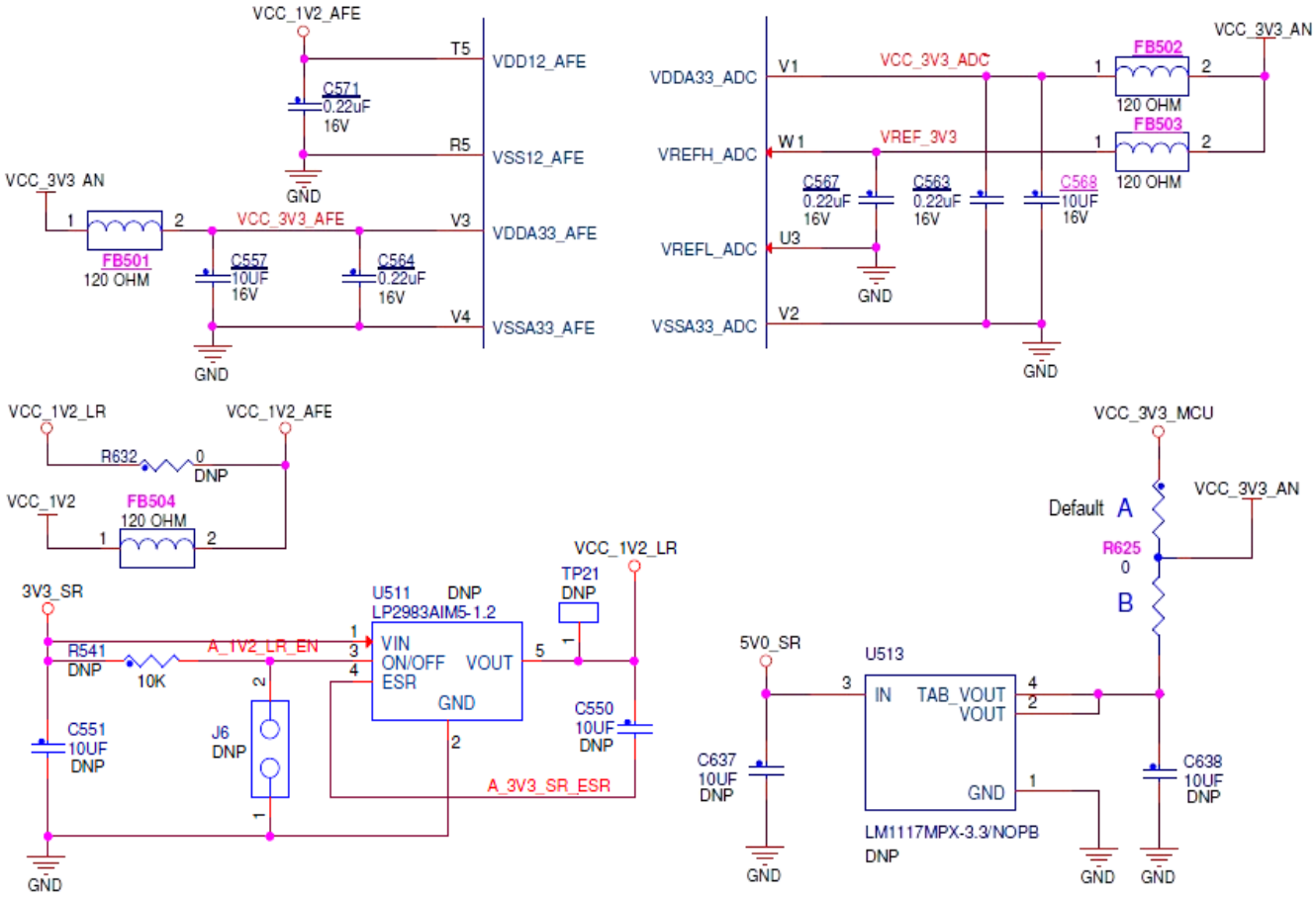

Figure 7. Analog MCU supplies

4.7 Measuring MCU power consumption

The EVB design provides means for measuring currents in the major MCU power rails.

4.7.1 Measuring main 3.3V current

Header J9 (see Figure 8 and Table 15) is intended for measuring current in the MCU 3.3V power rail. Diode DD2 in parallel to it guarantees the 3.3V power is uninterrupted even when J9 open.

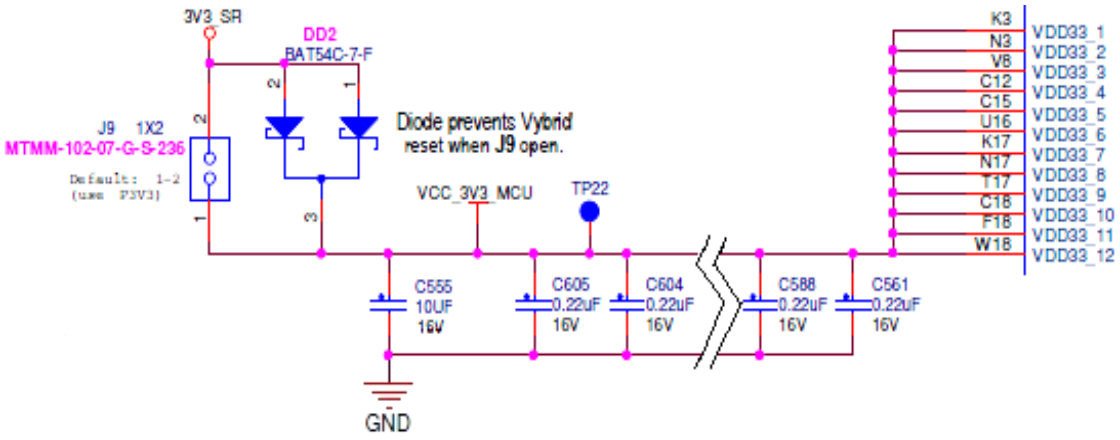

Figure 8. Measuring MCU 3.3V rail current

4.7.2 Measuring USB PHY current

Headers J4 and J7 controlling power for the MCU USB PHYs (see Section 11.4, "Dual USB interface (P1, P9)") may also be used to measure current if their jumpers are replaced with an ammeter (see Figure 21 and Table 15).

4.7.3 Measuring 1.2V current

Due to layout constraints, there is no dedicated header to measure the MCU 1.2V current, but it can be done if a 0-Ohm resistor in the R28 location (see Figure 6 and Table 15) is replaced with a current-sense one. For user's convenience, eight 0.02-Ohm 1% current-sense resistors are provided on the board (see Figure 9).

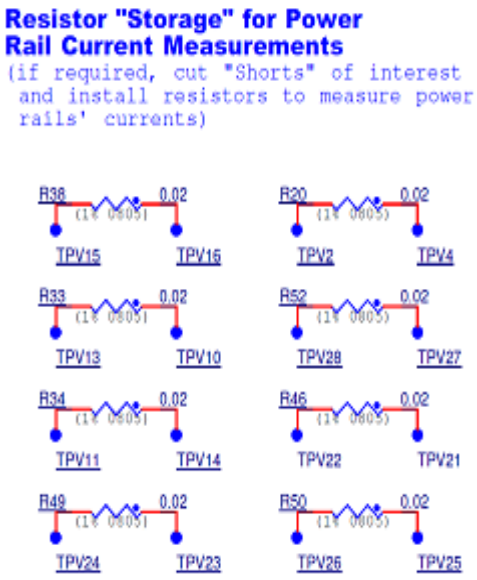

Figure 9. On-board current-sense resistors

4.7.4 Measuring currents in other power rails

Numerous power rails have series “shorts” (e.g., SH15 in the MPU SDRAM controller power rail)–exposed copper footprints consisting of two pads shorted with a trace. If required, the trace can be cut and a current-sense resistor soldered onto the pads.

Refer to the EVB-VF522R3 Schematic for details.

4.7.5 Powering EVB peripherals

The power-routing options detailed in Section 4.6, “MCU supply routing” only impact the voltage supply to the MCU and not any of the EVB peripherals. Power domains used by the EVB peripherals are shown in Table 2, which provides a reference to either disable a regulator or manually provide the voltage for that power domain.

Table 2. EVB peripherals power

Power Domain	Used On
12V	MLB daughtercard connector
5V Switch-Mode	CAN transceiver Board-to-Board MAC (Ethernet) connector USB circuitry DCU daughtercard connector Radio Tuner daughtercard connector Generic CD connector LCD connector (header)

Table 2. EVB peripherals power

3.3V Switch-Mode	MCU reset circuitry External 24 MHz oscillator (optional) Peripheral reset-control multiplexer Mode configuration (BOOTMOD[0..1] and RCON[0..31] pull-up resistors) Debug (JTAG and Cortex) headers CAN transceiver LIN transceiver SCI transceiver Board-to-Board MAC (Ethernet) connector USB circuitry QuadSPI Flash SD connector DCU daughtercard connector MLB daughtercard connector Push button preset switches Audio DSP circuitry (directly and via 3V3_Audio) SPI Serial Flash (optional usage) “Aux In” audio ADC circuitry (via 3V3_Audio) Microphones Left & Right (via 3V3_Audio) Audio DACs (via 3V3_Audio) Radio Tuner daughtercard connector Generic CD connector Bluetooth daughtercard connector I^2C daughtercard connector
1.5V Switch-Mode	DDR3 SDRAM circuitry
3.3V Linear	ADC potentiometer
1.8V Linear	DCU daughtercard connector Audio DSP circuitry Headphone amplifiers (via 1V8_Audio)

5 Clocking scheme

There are three on-board clock sources available–a crystal-based (Y4) 32.768 kHz MCU built-in oscillator and two 24 MHz ones:

- Crystal-based (Y3) MCU built-in oscillator used on the EVB by default (with R621 configured as per Table 15),
- Optional external oscillator (Y2), and Figure 10 demonstrates how its 3.3V-rated output is connected to a 1.1V-rated MCU input for applications requiring a high-quality clock source.

When Y2 is used, the Y3-based circuit (Y3, C63, C66, and R640) shall be unpopulated.

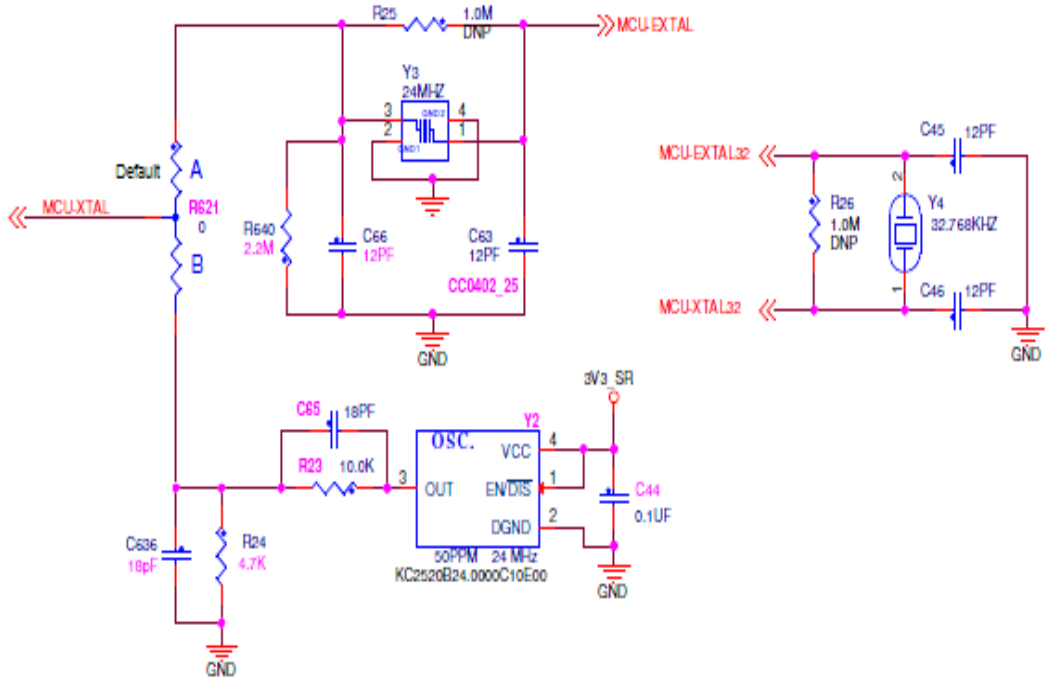

Figure 10. On-board clock options

The MCU device also features two fully internal reference clocks (IRC):

- Fast (24 MHz),
- Slow (128 kHz); the signal is divided by 4 by default to provide an internal 32 kHz clock to the device.

6 MCU reset block

The MCU reset block has the following features (see Figure 11):

- Active-low open-drain output with status LED (DS2),
- 3.3V-based power-on reset with ~ 200ms active timeout (delay),
- Manual reset (using SW7),
- Reset caused by the JTAG TRST signal (see Section 9, “Debug interfaces (P15, P16)”).

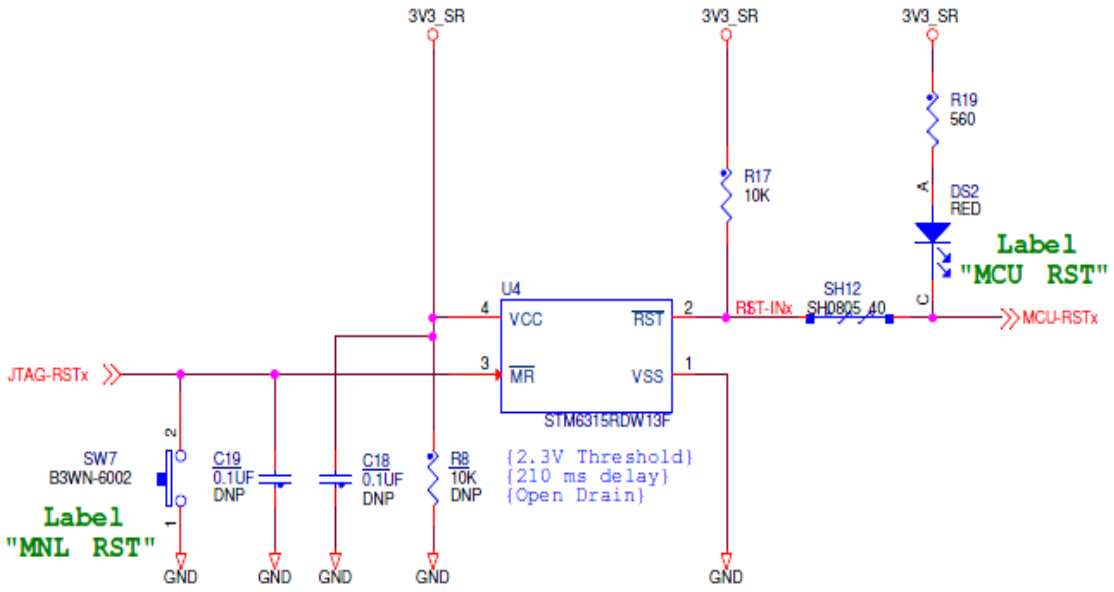

Figure 11. MCU reset block

7 Peripheral reset-control multiplexer

The EVB includes an 8-output multiplexer (U8) to reset the major peripherals (see Figure 12). Its outputs are of a push–pull type (except for the unused open-drain Output 0).

When reset, all the outputs are in the high-impedance state; however, thanks to pull-down resistors on the used outputs, the controlled peripherals are staying in the reset state until the outputs are actively driven by the MCU over the I^2C bus (address 0x30).

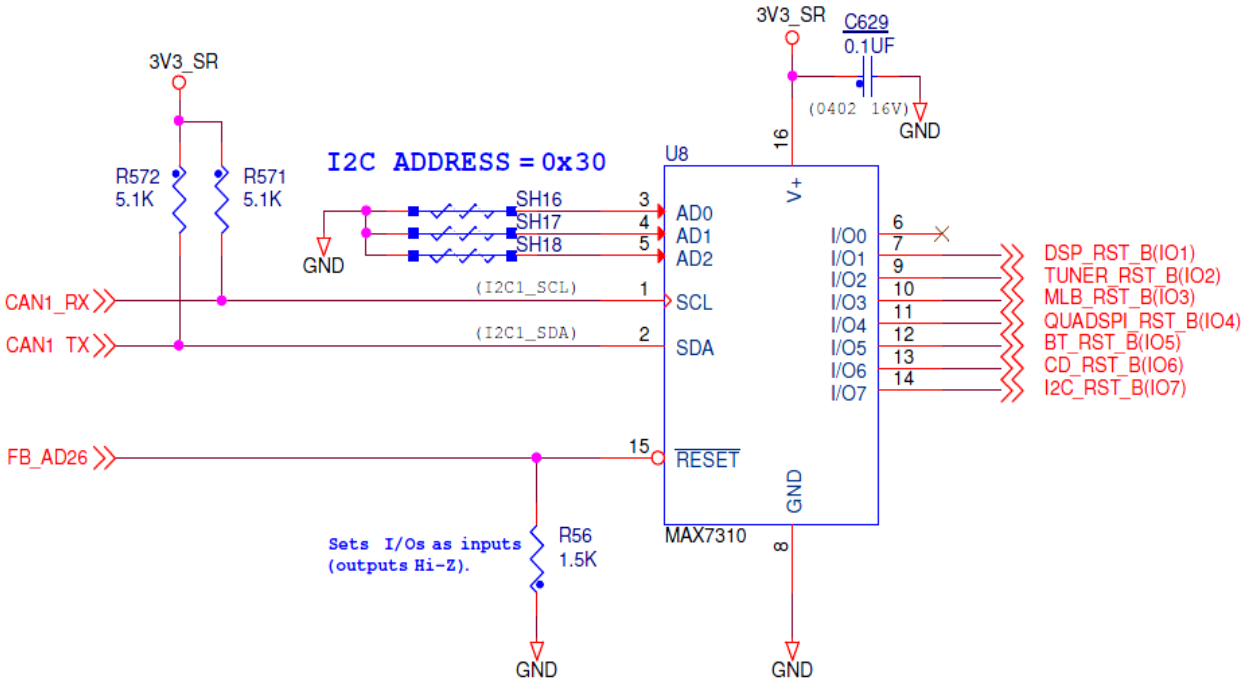

Figure 12. Peripheral reset-control multiplexer

8 MCU reset boot configuration

8.1 Boot mode selection (J14, J15)

Vybrid has two boot-mode pins (BOOTMOD[0..1]) routed to jumpers J14 and J15 to determine the EVB boot behavior (see Table 15). By default, boot configuration will be read from the internal fuses.

8.2 RCON configuration (SW8 to SW11)

In addition, there are 32 switches (four 8-way miniature slide switches as per Figure 13), which can be used to setup the Vybrid RCON pins behavior prior to blowing its internal boot fuses (see Table 3), the ON switch position meaning “Logic High” on the RCON pin.

Reset configuration is read from the RCON switches when BOOTMOD[0..1] is set to 10 and ignored for the rest of the values (see Table 15).

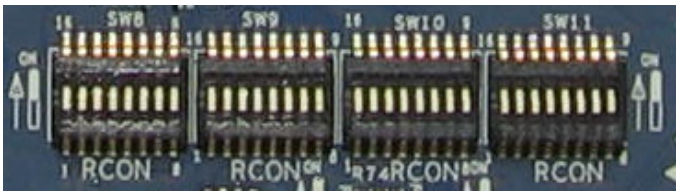

Figure 13. RCON slide switches

Table 3. RCON switches

Switch	RCON Bits
SW11[8..1]	RCON[31..24]
SW10[8..1]	RCON[23..16]
SW9[8..1]	RCON[15..8]
SW8[8..1]	RCON[7..0]

9 Debug interfaces (P15, P16)

Two debugging JTAG headers are provided on the EVB-VF522R3 board (pinout shown in Figure 14, Table 4, and Table 5):

- Standard 20-pin (P15)
- Cortex 10-pin (P16)

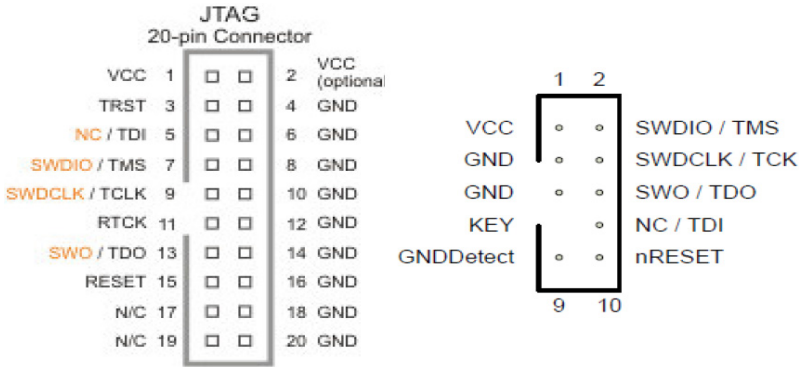

Figure 14. Debug headers

Table 4. Standard debug header (P15)

Signal	Function	Pin No	Pin No	Function	Signal
3V3	VCC (Debug VREF)	1	2	VCC (Debug VREF)	3V3
---	nTRST	3	4	GND	GND
JTDI	TDI	5	6	GND	GND
JTMS	TMS	7	8	GND	GND
JTCLK	TCLK	9	10	GND	GND
GND	RTCK	11	12	GND	GND
JTDO	TDO	13	14	GND	GND
JTAG-RST	nSRST	15	16	GND	GND
---	NC	17	18	GND	GND
---	NC	19	20	GND	GND

Table 5. Cortex debug header (P16)

Signal	Function	Pin No	Pin No	Function	Signal
3V3	VCC (Debug VREF)	1	2	TMS	JTMS
GND	GND	3	4	TCLK	JTCLK
GND	GND	5	6	TDO	JTDO
---	Key	7	8	TDI	JTDI
---	---	9	10	nSRST	JTAG-RST

10 On-board memory

This section details configuration of the on-board memories:

- DDR3 SRAM (U6)
- QuadSPI Flash (U507 to U509)
- SD card socket (P500)

10.1 DDR3 memory

- A single 1 Gb (64Mx16) DDR3 memory chip in the 96-ball FBGA package (e.g. MT41J64M16 by Micron Technology) is installed on the EVB.
- It is powered from the above-mentioned (see Section 4.2, “Switch-mode voltage regulator (U7)”) 1.5V power rail (along with the ballast transistor Q2).
- A simple resistor divider is good enough to generate the 0.75V DDR3 reference (see Figure 15).

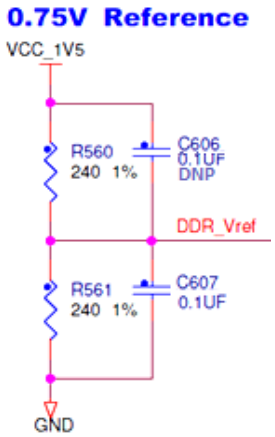

Figure 15. DDR3 0.75V reference supply

- The EVB is laid out so that it needs no external termination resistors, which simplifies its design and lowers power consumption.
- DDR3 self-refresh (low-power) mode is supported even when Vybrid is in any of the LPSTOPx modes, in which its I/Os are switched into a high-impedance mode. The on-board pull-up on DDR_RESET and pull-down on DDR_CKE lines keep the DDR3 chip in self-refresh mode.

10.2 QuadSPI memory

Three 256 Mb (32MB) Quad-I/O Serial Flash memory chips (e.g. S25FL256S by Spansion) are installed on the EVB:

- Flash A connected to Vybrid QSPI0_A interface
- Flash B connected to Vybrid QSPI0_B interface
- Flash C connected to Vybrid QSPI1_A interface

The memory type installed does not use the Vybrid DQSx signal lines, so these are disconnected by default and Vybrid uses them as GPIOs.

Refer to the EVB-VF522R3 Schematic for details.

The following Vybrid features can be implemented on the EVB:

- QuadSPI eXecute-In-Place (XiP) mode
- Both Single (SDR) and Dual Data Rate (DDR)
- Parallel QuadSPI operation in DDR mode
- Using QuadSPI memory as a boot device by the internal Boot ROM

NOTE

The QuadSPI memory reset input is connected to output 4 of the peripheral reset-control multiplexer (see Section 7, “Peripheral reset-control multiplexer”). When reset, its outputs are in the high-impedance state, but, thanks to a pull-down resistor on the reset line, the QuadSPI memory is reset until the line is actively driven by the MCU via the peripheral reset-control multiplexer.

10.3 SD card interface

The EVB features an SD card interface:

- The Vybrid MCU device has two SD host controllers, SDHC0 & SDHC1.
- SDHC1 is connected to a SD card slot.
- SDHC0 is not used due to that some of its shared pins are already used for other functions.
- SD card detection is via a request on pin 2 rather than a mechanical switch.
- A SD card can be used as a boot device by the internal Vybrid Boot ROM.

11 Communication interfaces

11.1 CAN interface (P23, P24, P27)

The EVB features a high-speed CAN bus interface (see Figure 16):

- On the digital side, connected to MCU CAN0,
- On the media side:

— Connected to a 4-pin 0.1” 1x4 header (P27),
— Optional on-board termination via a 2-pin header (P23 as per Table 15),
— Optional 12V power via a 2-pin header (P24 as per Table 15).

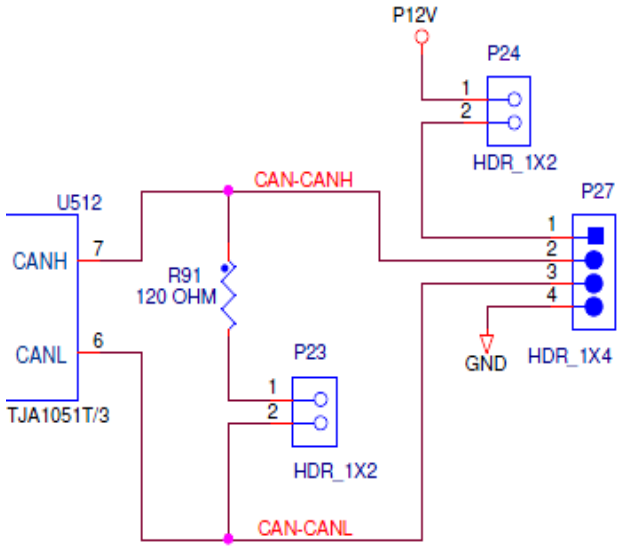

Figure 16. CAN physical interface connector

11.2 SCI/LIN interface (J16, J17, P21, P25, P26)

The Vybrid SCI0 channel is shared on the EVB by the two serial interfaces - SCI and LIN, selection being provided by jumpers J16 and J17 (see Table 15).

11.2.1 SCI configuration (P26)

To provide signal translation, the EVB SCI interface has a RS232 transceiver (U10), which is:

- Connected to a standard 9-way female D-type connector (P26) allowing a direct connection to a PC or terminal, pinout being shown in Figure 17,
- Providing no hardware flow control support.

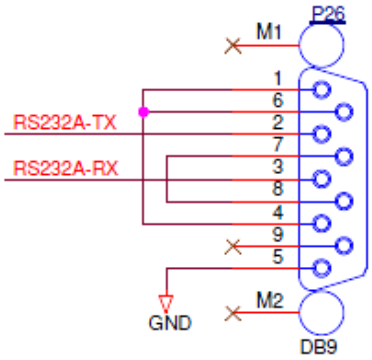

Figure 17. RS232 physical interface connector

11.2.2 LIN configuration (P21, P25)

To provide signal translation, the EVB LIN interface (see Figure 18) has a transceiver (U9), which is:

- Configured as Master by default (for Slave mode, remove resistor R79 as per Table 15),
- Connected to a standard 4-pin Molex connector (P25) shown in Figure 19 and used on most other Freescale EVBs supporting LIN,
- Powered either from LIN line or from local 12V via the 2-pin header (P21 as per Table 15).

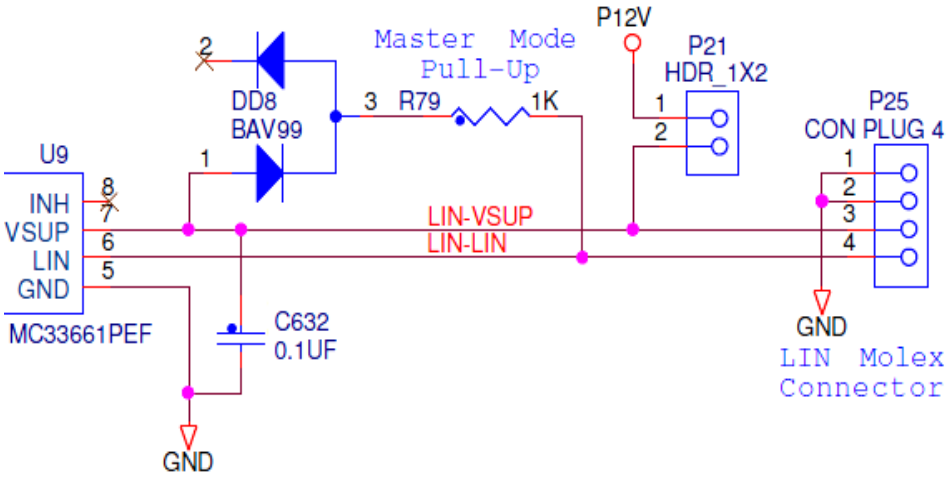

Figure 18. LIN physical interface

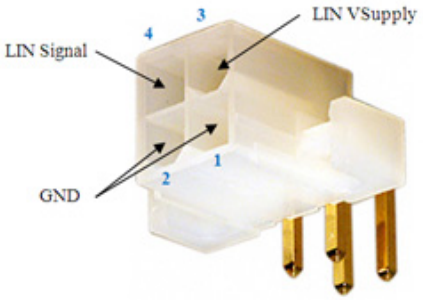

Figure 19. LIN Molex connector

11.3 MAC (Ethernet) interface (J10)

The installed Vybrid device features two MAC interfaces, #0 and #1, used as follows:

- #0 is used in the RMII (Reduced MII) mode and routed to a board-to-board connector (J10) with type and pinout defined in the DOC-01898 document; a relevant daughtercard, e.g. IMXAI2ETH-SMSC (see Figure 20), can be plugged into it,
- Pins of the other one are used for other functions

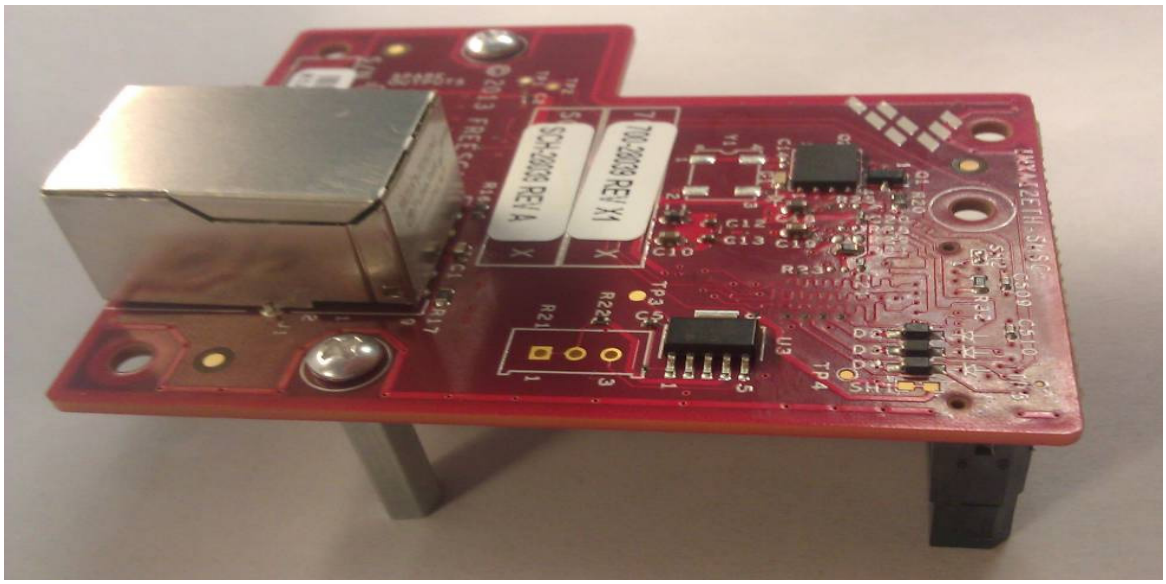

Figure 20. Ethernet daughtercard

11.4 Dual USB interface (P1, P9)

The installed Vybrid MCU device features two USB OTG ports with on-chip HS/FS/LS PHYs; they are connected to the below EVB ports with 0.5A power support each:

- USB0 - “On-The-Go Micro AB” connector (P9),
- USB1 - “Type A Host” connector (P1).

They are powered through jumpers J4 and J7 as shown in Figure 21, their configuration setting being described in Table 15.

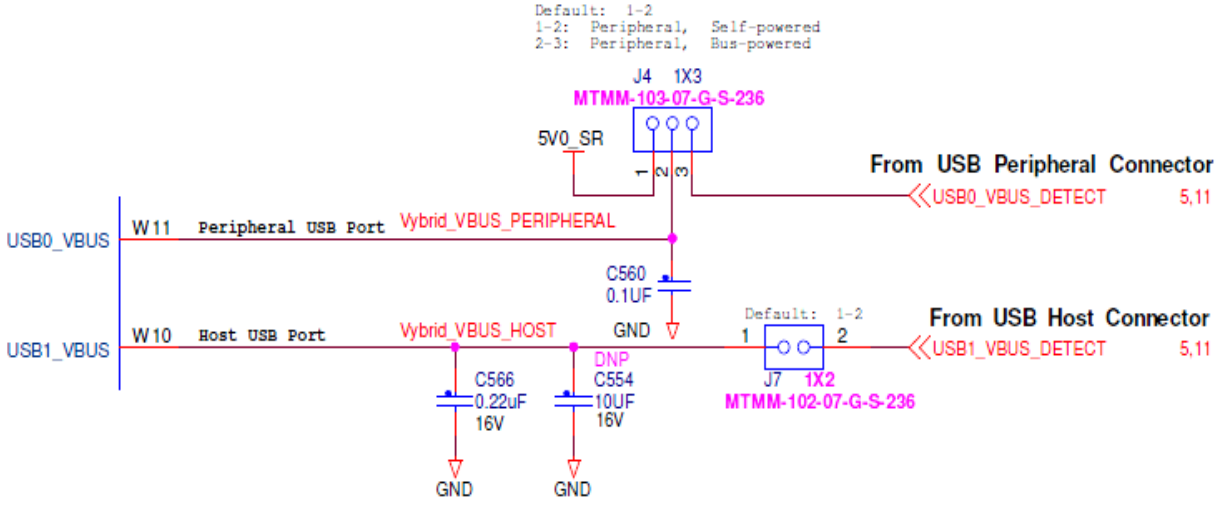

Figure 21. MCU USB interfaces power

12 Video interfaces

The EVB has camera input connectors as well as a DCU daughtercard connector, e.g. for connecting a display daughtercard.

12.1 Video inputs (P2 to P5)

There are four RCA “Phono” connectors routed to the MCU Video ADC inputs 0 to 3. They allow direct connection to a video source (camera, etc.) in a composite video format.

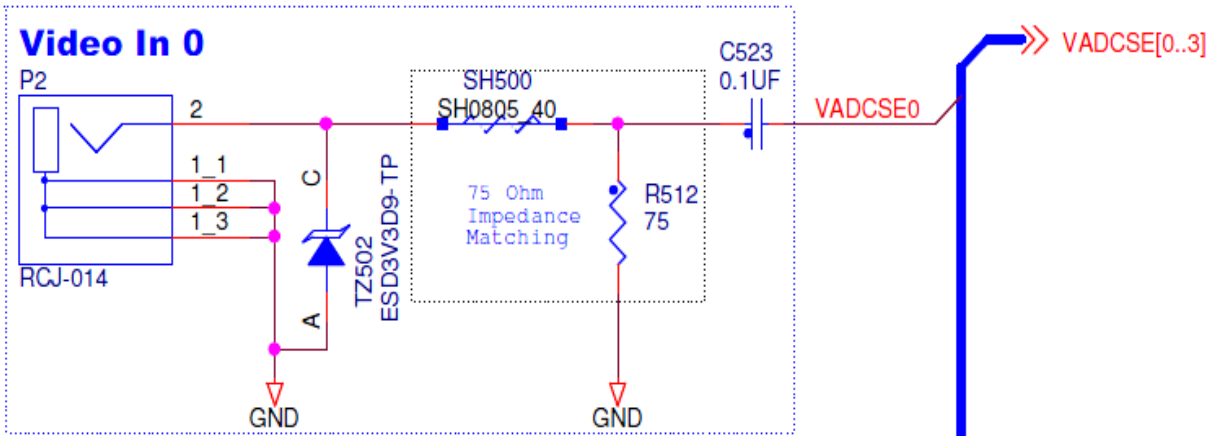

Figure 22. Video input

As illustrated on the Video Input 0 example in Figure 22, the impedance-matching circuit can be also used signal attenuation if zero resistance of the “short” footprint is replaced with a non-zero value and the R512 value lowered accordingly while keeping their sum equal 75 Ohms for matching with the 75-Ohm video cable plugged into P2.

12.2 Graphical device interface (P20)

A 120-pin connector P20 features a graphical device interface as well as various auxiliary signals. Thanks to its unified type and pinout, it matches:

- The Freescale TFT LCD daughtercards, e.g., the 7-inch LCD-WVGA-7IN-1 one,
- The Freescale HDMI daughtercards, e.g., MCIMXHDMICARD shown in Figure 23.

Figure 23. HDMI daughtercard

12.2.1 DCU interface

Out of the two Vybrid on-chip Display Control Unit (DCU) modules, primary DCU0 and secondary DCU1, only the former is used on the EVB; it features the following signals:

- RGB - DCU0_B0 to DCU0_B7, DCU0_R0 to DCU_R7, and DCU_G0 to DCU_G7,
- Synchronization - DCU0_HSYNC, DCU0_VSYNC, and DCU0_PCLK.

12.2.2 Power

Three power rails are provided - 1.8V, 3.3V, and 5V.

12.2.3 Touchscreen interface

Based on the MCU ADC functionality, a classic four-wire resistive touchscreen is supported.

12.2.4 I^2C interface (J18, J19)

Using jumpers J18 and J19, two out of the four above-mentioned touchscreen lines (see Section 12.2.3, “Touchscreen interface”) are shared on the connector P20 with the I^2C lines (see Table 15).

12.2.5 Auxiliary signals

P20 featured the following auxiliary signals:

- Reset (pull-down and optional pull-up resistors provided),
- Exposed power enable (pull-up resistor provided),
- Exposed display brightness (pull-up resistor provided),
- Optional LED interrupt indication, either Active High or Low - DS7 "DVI_DET_H" or DS8 "DVI_DET_L", respectively,
- HDMI - SCLK, SPDIF, SD0, and WS.

13 Audio blocks

The EVB features the following major audio blocks:

- Two miniature on-board microphones,
- “Aux In” port,
- Two headphone output ports.

Additionally, there is a generic CD header and Bluetooth daughtercard connector for remote audio detailed in Section 14.7, “CD header (P18)” and Section 14.8, “Bluetooth daughtercard header (J5)”, respectively.

13.1 Microphones

A stereo pair of miniature on-board microphones is:

- Placed at the bottom left (U503) and bottom right (U504) of the EVB,

- Addressable via the MCU channel SAI1.

13.2 “Aux In” connector (J1, P6)

A stereo “Aux In” port is implemented on a 3.5 mm jack socket P6. Its signal is fed through an input filter and then digitized in a dedicated audio ADC (U502) with the output routed to either the DSP (U510) or MCU EASI_SDI0 pin, depending on the jumper J1 configuration (see Table 15).

13.3 Headphone/audio outputs (P7, P8)

The EVB features two 3.5 mm stereo output jacks capable of load impedance as low as 32 Ohms, e.g. headphones. As shown in Figure 24, the stereo audio signal is fed from the DSP to a DAC (U505, U506), through a filter to the headphone amplifier (U501, U500) and finally to the output jack (P7, P8), respectively.

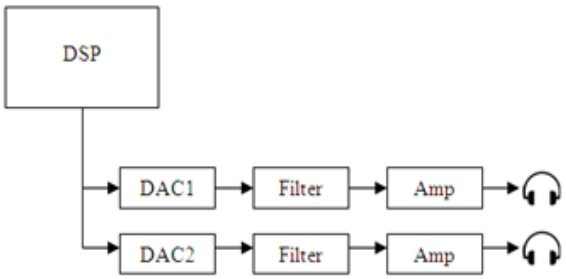

Figure 24. Audio output block

13.4 DSP block (J2, J3, P10)

The DSP block on the EVB:

- Is based on the DSP IC (U510),
- Has a dedicated DSP debug header (P10),
- Is capable of operation in both Slave (by default) and Master modes as selected by jumper J2 (see Table 15),
- Has a dedicated SPI Serial Flash IC (U2),
- Communicates with the MCU over the SPI0 (PCS0) channel,
- Boots either from the MCU or dedicated Flash.

NOTE

The DSP reset input is connected to output 1 of the Peripheral Reset-Control Multiplexer (see Section 7, “Peripheral reset-control multiplexer”). When reset, its outputs are in the high-impedance state, but, thanks to a pull-down resistor on the reset line, the DSP is reset until the line is actively driven by the MCU via the Peripheral Reset-Control Multiplexer.

13.4.1 Slave mode

This is a default mode of operation. This means that the DSP “firmware” is loaded to the DSP via the MCU SPI0 (PCS0) after boot.

13.4.2 Master mode

In this mode, using the dedicated debug header (P10) and DSP vendor’s programming tool and with a properly connected “Chip Enable” of the dedicated Flash (see Table 15 for the jumper J3 settings), the code for the DSP is loaded into the Flash, and the DSP will boot from it rather than the MCU SPI signals.

The SPI communication with the MCU, however, can still be configured such that the DSP acts as a Slave, i.e. all the necessary control (volume, effects, tone control, and so on) can still be controlled via the MCU.

Refer to the DSP documentation for details about its operation, programming, and configuring.

14 User I/O and control

There are various modules (available separately), switches, LEDs, connectors, and headers on the EVB as described in this section:

- 0.1” headers for MCU GPIO signals not used elsewhere (P11, P14),
- Potentiometer connected to the Vybrid ADC input (RV1),
- Two incremental encoders (SW1, SW2),
- Four dedicated station preset push buttons (SW3 to SW6),
- MLB daughtercard connector (P22),
- Radio tuner daughtercard connector (P13),
- I^2C daughtercard connector (P17),
- Generic CD header (P18),
- Bluetooth daughtercard connector (J5).

14.1 GPIO Headers (P11, P14)

There are two 0.1” pitch headers on the EVB for connecting to analog (P11) and digital (P14) GPIO signals, which are not used to directly drive other peripherals on the EVB (see Table 6 and Table 7).

Table 6. Connector P11 (analog)

Signal	Pin No		Pin No	Signal
ADC0SE8	1		2	ADC1SE8
ADC0SE9	3		4	ADC1SE9
DACO0	5		6	DACO1
REF_GND	7		8	REF_GND

Table 7. Connector P14 (digital)

Signal	Pin No		Pin No	Signal
FB_AD16	1		2	FB_AD17
FB_AD24	3		4	FB_AD25
FB_AD26	5		6	FB_AD29
FB_AD30	7		8	FB_AD31
SAI0_RX_BCLK	9		10	LVDSON
QSPI0_A_DQS	11		12	LVDSOP
QSPI0_B_DQS	13		14	FTM0CH5
GND (Digital)	15		16	GND (Digital)

NOTE

Some of the digital I/O signals are still used elsewhere on the EVB, so you must check availability prior to use. The signal cross-reference Table 14 should help with that.

14.2 ADC input potentiometer (RV1, TP8)

Useful for quick ADC testing, there is a small potentiometer (variable resistor) RV1 on the EVB, which routes a voltage between 0V and 3.3V into the MCU ADC input (pin ADC0SE8). An optional test point TP8 on this line can be used for voltage-monitoring purposes.

14.3 Radio control buttons

14.3.1 Incremental encoders (SW1, SW2)

There are two incremental rotary encoders on the EVB (24 clicks/12 pulses per rotation) with center push switch. These are intended to be used for radio development allowing volume/mode control.

The encoders are connected to the Vybrid FlexTimer Quad Decode channels for the rotation detection and to a GPIO for the center button push (see Table 8).

Table 8. Incremental encoders

Encoder	GPIO	FTM Channels
SW1	FB_AD24	CHA – FB_AD19 (QD_PHA) CHB – FB_AD18 (QD_PHB)
SW2	FB_AD25	CHA - FTM1CH0 (QD_PHA) CHB - FTM1CH1 (QD_PHB)

14.3.2 Radio preset buttons (SW3 to SW6)

There are four active-high push buttons connected to GPIOs as shown in Table 9). These can be used as general purpose switches or for radio presets should this hardware be used for a car radio development.

Table 9. Radio preset buttons

Switch	Preset No	Respective MCU Pin
SW4	1	FB_AD31
SW6	2	FB_AD30
SW5	3	FB_AD29
SW3	4	SAI0_RX_SYNC

14.4 MLB daughtercard connector (P22)

There is a 40-pin MLB (Media Local Bus) interface connector (P22) on the EVB for connecting a daughtercard shown in Figure 25). There are no hardware configuration options on the EVB in relation to the MLB card.

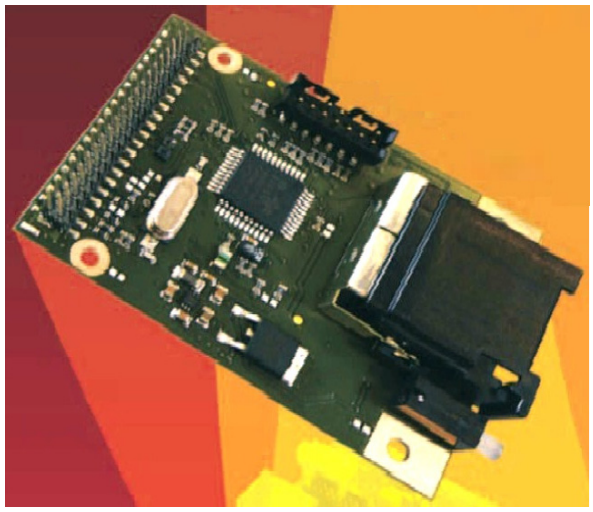

Figure 25. MLB daughtercard

NOTE

The daughtercard Reset input is connected to output 3 of the Peripheral Reset-Control Multiplexer (see Section 7, “Peripheral reset-control multiplexer”). When reset, its outputs are in the high-impedance state, but, thanks to a pull-down resistor on the reset line, the daughtercard is reset until the line is actively driven by the MCU via the Peripheral Reset-Control Multiplexer.

CAUTION

Ensure that the EVB is powered OFF prior to fitting or removal of the daughtercard.

14.5 Radio tuner daughtercard connector (P24)

The EVB has a connector to allow a Silicon Labs radio tuner daughtercard (see Figure 26) to be fitted. There are no hardware configuration options on the EVB in relation to the tuner card.

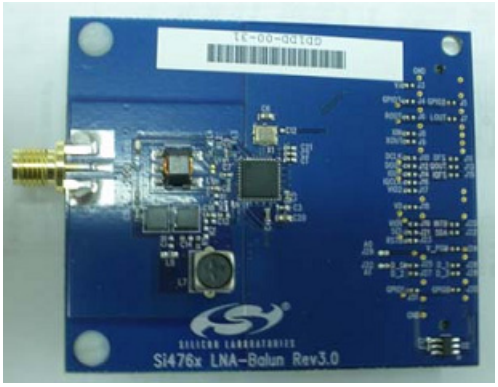

Figure 26. Radio tuner daughtercard

NOTE

The daughtercard Reset input is connected to output 2 of the Peripheral Reset-Control Multiplexer (see Section 7, "Peripheral reset-control multiplexer"). When reset, its outputs are in the high-impedance state, but, thanks to a pull-down resistor on the reset line, the daughtercard is reset until the line is actively driven by the MCU via the Peripheral Reset-Control Multiplexer.

CAUTION

Ensure that the EVB is powered OFF prior to fitting or removal of the daughtercard.

14.6 I²C Connectors and headers

Refer to the EVB-VF522R3 Schematic for details.

14.6.1 I²C Daughtercard connector with 3.3V power (P17)

A 10-pin 0.1" pitch connector (P17) enables connection of a custom-made 3.3V-powered daughtercard supporting various applications and matching the connector type and pinout (see Table 10).

Table 10. I²C daughtercard connector

Signal	Function	Pin No
FB_AD28	I²C SCL	1
FB_AD27	I²C SDA	3
3V3	VCC	5
---	---	7
---	---	9

Pin No	Function	Signal
2	GND	GND
4	---	---
6	---	---
8	Reset	I²C_RST
10	---	---

NOTE

The daughtercard Reset input (acting as Chip Select when applicable) has a pull-down resistor but, as an option, may be connected to output 7 of the Peripheral Reset-Control Multiplexer (see Section 7, "Peripheral reset-control multiplexer").

CAUTION

Ensure that the EVB is powered OFF prior to fitting or removal of the daughtercard.

14.6.2 I²C header with 5V power (P19)

A 4-pin 0.1-inch pitch header (P19) enables connection of a custom-made 5V-powered daughtercard supporting various applications and matching the connector type and pinout (see Table 11).

Table 11. I²C header

Signal	Function	Pin No	Pin No	Function	Signal
5V0	VCC	1	2	I²C SDA	I²C3_SDA
GND	GND	3	4	I²C SCL	I²C3_SCL

CAUTION

Ensure that the EVB is powered OFF prior to fitting or removal of the daughtercard.

14.7 CD header (P18)

There is a 0.1-inch pitch generic CD header fitted on the EVB as described in Table 12.

Table 12. Generic CD header

Signal	Pin No	Pin No	Signal
3.3V	1	2	5.0V
SAI2_RX_BCLK	3	4	I²C3_SCL
SAI2_RX_DATA	5	6	I²C3_SDA
SAI2_RX_SYNC	7	8	---
RESET	9	10	MCLK (from DSP)
GND	11	12	GND

NOTE

The daughtercard Reset input is connected to output 6 of the Peripheral Reset-Control Multiplexer (see Section 7, "Peripheral reset-control multiplexer"). When reset, its outputs are in the high-impedance state, but, thanks to a pull-down resistor on the reset line, the daughtercard is reset until the line is actively driven by the MCU via the Peripheral Reset-Control Multiplexer.

CAUTION

Ensure that the EVB is powered OFF prior to fitting or removal of the daughtercard.

14.8 Bluetooth daughtercard header (J5)

The EVB includes a 0.1-inch pitch 30-pin header (see Table 13) to allow connection of a Freescale-designed Bluetooth daughtercard (P/N FD-B-TOOTH-DC) shown in Figure 27.

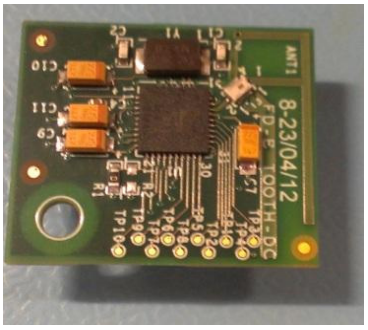

Figure 27. Bluetooth daughtercard

Table 13. Bluetooth daughtercard header

Signal	Pin No	Pin No	Signal
SAI0_RX_DATA	1	2	SAI0_TX_BCLK
SAI0_TX_SYNC	3	4	---
---	5	6	SAI0_TX_DATA
---	7	8	SCI0_TX
SCI0_RX	9	10	SDHC1_CLK
---	11	12	SCI0_CTS
SCI0_RTS	13	14	SDHC1_CMD
---	15	16	FB_AD20 (SDHC1_CD)
RESET	17	18	---
SDHC1_A_DATA0	19	20	SDHC1_DATA1
SDHC1_A_DATA2	21	22	SDHC1_DATA3
---	23	24	---

Table 13. Bluetooth daughtercard header

Signal	Pin No	Pin No	Signal
---	25	26	---
GND	27	28	3.3V
GND	29	30	GND

NOTE

The daughtercard Reset input is connected to output 5 of the Peripheral Reset-Control Multiplexer (see Section 7, "Peripheral reset-control multiplexer"). When reset, its outputs are in the high-impedance state, but, thanks to a pull-down resistor on the reset line, the daughtercard is reset until the line is actively driven by the MCU via the Peripheral Reset-Control Multiplexer.

CAUTION

Ensure that the EVB is powered OFF prior to fitting or removal of the daughtercard.

15 MCU I/O connections and pin usage

Table 14 provides a useful cross-reference to see what MCU port pins are used and shared by the various EVB peripherals and functions.

Table 14. Pin usage and sharing

EVB Function	1st Used Function of MCU Pin(s)	2nd Used Function of MCU Pin(s)	Shared with EVB Function(s)
Peripheral Reset-Control	I^2C1_SDA	CAN1_TX	Touchscreen, Tuner
	I^2C1_SCL	CAN1_RX	Touchscreen, Tuner
	Reset Control	FB_AD26	P14 (unused digital GPIOs)
Boot Mode	BOOTMOD[0]	DCU0_VSYNC	DCU
	BOOTMOD[1]	DCU0_HSYNC	DCU
RCON	RCON[0..17]	DCU0_R/G/B[2..7]	DCU
	RCON[18..20]	RMII0_x	MAC (Ethernet)
	RCON[21,23]	SAI0_x	Bluetooth
	RCON22	SAI0_RX_SYNC	Preset SW3
	RCON[24..29]	SAI1_x (all)	DSP (including dedicated Flash), Microphones, Touchscreen
	RCON[30..31]	FTM0CH[1..2]	QuadSPI1 (Flash C)

Table 14. Pin usage and sharing

EVB Function	1st Used Function of MCU Pin(s)	2nd Used Function of MCU Pin(s)	Shared with EVB Function(s)
JTAG, Cortex	TCK, TDO, TMS	---	MLB
CAN	CAN0 (TX, RX)	---	---
LIN / SCI	SCI2 (TX, RX)	FB_AD[22,23]	---
MAC (Ethernet)	RMII0 (all)	---	RCON[18..20]
	GPIO (for optional interrupt)	---	Tuner
USB0 (Type A Host)	USB0_x	---	---
USB1 (OTG Type AB)	USB1_x	---	Optionally SD
DDR3	DDR_x	DDR_x	---
QuadSPI0 (Flash A)	QSPI0_A_x	QSPI0_A_x	Unused DQS on P14 (unused digital GPIOs)
QuadSPI0 (Flash B)	QSPI0_B_x	QSPI0_B_x	Unused DQS on P14 (unused digital GPIOs)
QuadSPI1 (Flash C)	FTM0[0..5]	QSPI1_A_x	RCON[30,31] (FTM0CH[1..2]), unused FTM0CH5 (DQS) on P14 (unused digital GPIOs)
SD	SDHC1_x	---	Optionally USB1 (OTG Type AB)
RCA Video In	VADCSE[0..3]	VADCSE[0..3]	---
DCU	DCU0_x	---	RCON[0..17] (DCU0_R/G/B[2..7])
DCU I^2C	CAN1_x	CAN1_x	Peripheral Reset-Control, Tuner (I^2C1)
Touchscreen	SAI1_x, RMII1_x	---	RCON[27,29]
MLB	JTAG (TCK, TDO, TMS)	---	JTAG, Cortex
	FB_ADx	---	P14 (FB_AD[16,17])
	I^2C3_x	---	Generic CD, 4-pin header, and MAC (Ethernet)
ADC Potentiometer	ADC0SE8	---	P11 (unused analog GPIOs)
Left Encoder	FTM1CH[0..1]	---	---
	FB_AD25	GPIO	P14 (unused digital GPIOs)
Right Encoder	FB_AD[18,19]	---	
	FB_AD24	GPIO	P14 (unused digital GPIOs)
Preset Switches	FB_AD[29..31]	GPIO	P14 (unused digital GPIOs)
	SAI0_RX_SYNC	GPIO	RCON22

Table 14. Pin usage and sharing

EVB Function	1st Used Function of MCU Pin(s)	2nd Used Function of MCU Pin(s)	Shared with EVB Function(s)
"Aux In" dedicated audio ADC	RMII1_[MDC, MDIO]	ESAI_x	DSP, Tuner
	DSPI0_PCS1	AUDIO_MCLK	Audio DACs, DSP
Microphones (Left & Right)	SAI1_RX_[BCLK, SYNC, DATA]	---	RCON[25,26,28]
DSP	Various	Various	EASI (Tuner, audio ADC), AUDIO_MCLK (audio DACs and ADC), SAI1_TX_BCLK (RCON24)
DACs for Audio Outputs	DSPI0_PCS1	AUDIO_MCLK	Audio ADC, DSP
Tuner	RMII1_[MDC, MDIO]	EASI_x	Audio ADC, DSP
	CAN1_x	I^2C1_x	DCU I^2C, Peripheral Reset-Control
	GPIO (for interrupt)	---	Optionally MAC (Ethernet)
3.3V-powered I^2C	FB_AD[27,28]	I^2C2_[SCL,SDA]	---
Generic CD	I^2C3_[SDA,SCL]	---	5V-powered I^2C, MAC (Ethernet), MLB
	SAI2_[BCLK, SYNC, DATA]	---	---
Bluetooth	SAI0_TX_[DATA, SYNC]	RCONx	RCON[21,23]
	SCI0_TX	---	---
	SDHC_[CLK,CMD,DATA1,DATA3], FB_AD20	---	SD

NOTE

Some active signals, i.e. I^2C, can be shared by several peripherals without any problems.

16 Configuration settings

Table 15 shows available settings of the configuration devices on the EVB. The default settings shown in **bold text** should allow a more rapid return to the default EVB state if required.

Table 15. Configuration settings

Device	Function	Position	Legend	Description
J1	"AUDIO IN" ADC routing	**1-2**	**1**	**To MCU**
		2-3	3	To DSP
		Removed	---	To none

Table 15. Configuration settings

J2	DSP mode of operation	1-2		1	Slave (from MCU)
		2-3		**3**	**Master (from SPI Serial Flash)**
J3	DSP Flash “Chip Enable” control	1-2		1	By MCU (for DSP Slave mode)
		2-3		**3**	**By DSP & DSP debug header (for Master mode)**
J4*	MCU USB0 PHY power source	**1-2**		**1**	**Self-powered**
		2-3		3	Bus-powered (from P9)
		Removed		---	Unpowered
J6	Optional 1.2V linear regulator output control	**Removed**		---	**Enabled**
		Fitted		---	Disabled
J7*	MCU USB1 PHY power control	**Fitted**		---	**Powered**
		Removed		---	Unpowered
J8	MCU VBAT power source	**1-2**		**1**	**From main MCU 3.3V rail**
		2-3		3	From backup battery
		Removed		---	Unpowered
J9*	Main 3.3V power for MCU	**Fitted**		---	**Provided**
		(Removed)		---	(Not recommended)
J14, J15	MCU Boot Mode	J15 (MOD[1])	J14 (MOD[0])	BOOTMOD[1..0]	Boot Mode
		1-2 (Low)	1-2 (Low)	00	Internal fuses
		1-2 (Low)	2-3 (High)	01	Serial Download
		2-3 (High)	**1-2 (Low)**	**10**	**RCON Switches**
		2-3 (High)	2-3 (High)	11	(Reserved)
J16, J17	Transceiver selected	**1-2**		**1 / SCI**	**SCI (RS232)**
		2-3		3 / LIN	LIN
		Removed		---	None selected
J18, J19	Interface selected	**1-2**		**1**	**Touchscreen**
		2-3		3	I^2C
		Removed		---	None selected
P21	LIN interface power source	**Removed**		---	**From Molex connector**
		Fitted		---	Local
P23	CAN termination control	**Removed**		---	**OFF**
		Fitted		---	ON
P24	Power from EVB over CAN cable	**Removed**		---	**OFF**
		Fitted		---	ON

Table 15. Configuration settings

R28	MCU core ballast transistor collector voltage	**A**	---	**1.5V**
		B	---	3.3V
R79	LIN interface mode of operation	**Populated**	---	**Master**
		Removed	---	Slave
R621	MCU 24 MHz clock source	**A**	---	**MCU crystal oscillator**
		B	---	From external oscillator
R625**	MCU analog 1.2V power source	**A**	---	**From main MCU 1.2V power rail**
		B	---	From linear regulator
R632**, FB504**	MCU analog 3.3V power source	FB504	---	**From main MCU 3.3V power rail**
		R632	---	From linear regulator
SW8	MCU RCON (Reset CONfiguration)			**"RCON Switches" MCU Boot Mode** (ignored in all other MCU Boot Modes)
SW9				
SW10				
SW11				

Notes:

** Can be used for current measurements if replaced with a current measuring device.*

*** Can be used for current measurements if replaced with a current-sense resistor.*

Default settings for jumpers only are shown in Figure 28.

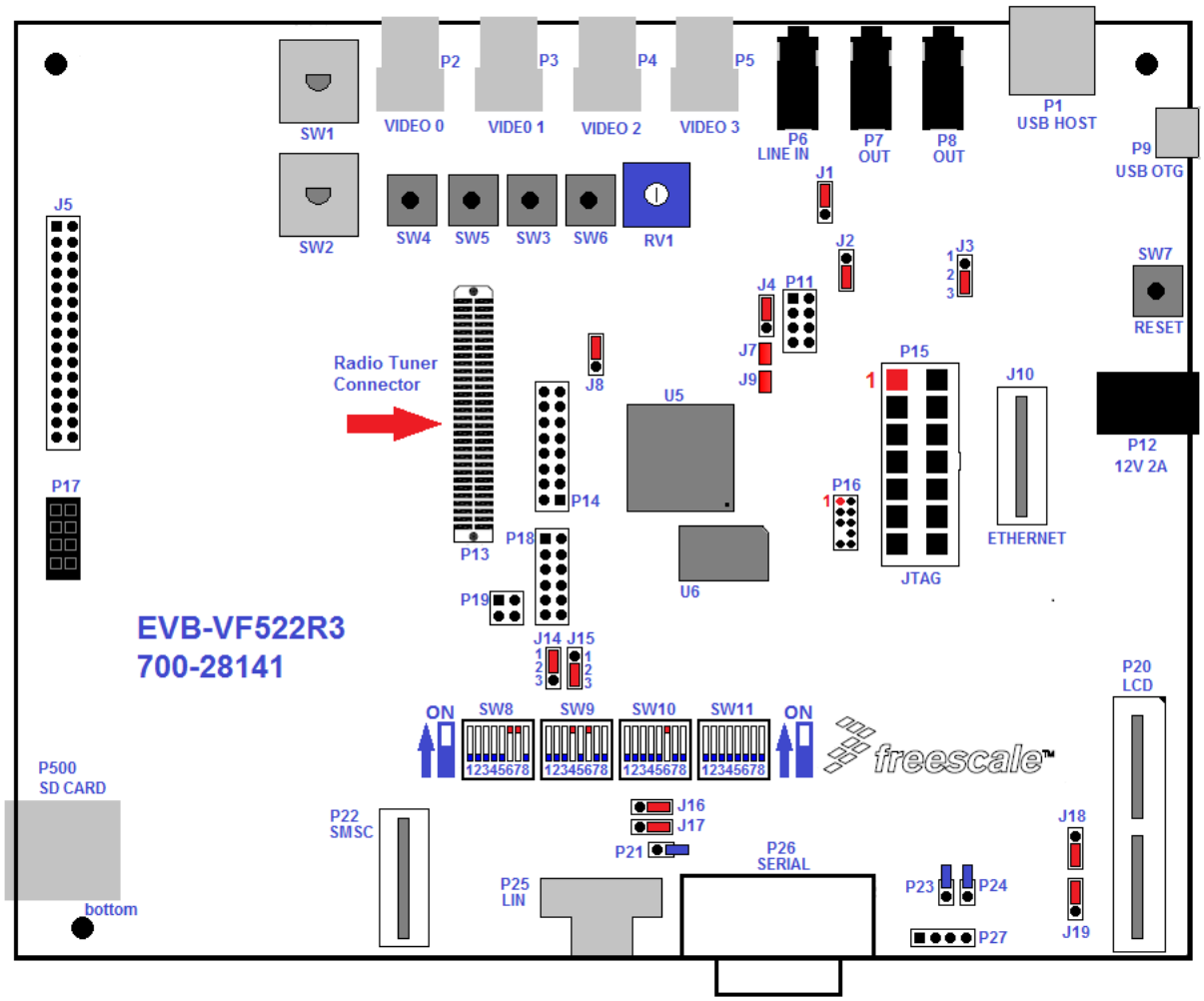

Figure 28. Default jumper settings

17 Getting started

To get started, follow steps provided in the EVB-VF522R3 Quick Start Guide.

18 Reference documents

More information on the Vybrid family and EVB System is provided in the documents below, which can be found in the documentation sections of freescale.com/Vybrid and freescale.com/EVB-VF522R3.

- VYBRIDVF6FS: Vybrid Family Fact Sheet,
- VYBRIDRM: Vybrid Reference Manual,
- VYBRIDSRM: Vybrid Security Reference Manual,
- EVB-VF522R3-QSG: Quick Start Guide
- EVB-VF522R3-SCH: Schematic
- EVB-VF522R3-PWB: Design Package

- DOC-01898: Ethernet Board-to-Board Connector Assignment.

19 Revision history

Revision	Date	Comment
0	11/2014	Initial Release

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