

Graphics Video Sync Adder/Extractor

General Description

The MAX9539/MAX9540 chipset provides a 3-wire (RGB) interface for 5-wire (RGBHV) video by adding and extracting the H, V, and composite sync from the graphics video signals. This chipset eliminates the problem of sync-to-video timing (skew errors) in a 5-wire interface, while reducing the number of channels required to transport video signals.

The MAX9539 mixes the H and V sync signals and adds them to create a 3-wire interface from a 5-wire (RGBHV) input. The MAX9540 recovers the H and V sync signals to create a 5-wire (RGBHV) interface from the 3-wire input. The MAX9540 also provides a composite sync output.

The chipset includes the MAX9539 sync adder and the MAX9540 sync extractor with 180MHz large-signal bandwidths to address display resolutions up to 1600 x 1200 at 85Hz for VGA-to-UXGA applications. Both devices feature a DC restore function, which virtually eliminates any changes in black level. The chipset uses a proprietary H and V sync addition/extraction scheme (true sync) to minimize skew errors.

The MAX9539/MAX9540 are available in 28-pin TSSOP packages and are specified over the extended -40°C to +85°C temperature range.

Applications

Enterprise Class (Blade) Servers
Laptop PCs
Web Appliances
Keyboard-Video-Mouse (KVM)

Features

- ◆ 3-Wire RGB to 5-Wire RGBHV Interface
- ◆ Supports VGA-to-UXGA Resolution
- ◆ Low Offset Voltage ($\pm 1\text{mV}$)
- ◆ 180MHz Large-Signal Bandwidth

Ordering Information

| PART | PIN-PACKAGE | PKG CODE | DESCRIPTION |
|--------------|-------------|----------|----------------|
| MAX9539EUI+* | 28 TSSOP | U28-3 | Sync Adder |
| MAX9539EUI | 28 TSSOP | U28-3 | Sync Adder |
| MAX9540EUI+* | 28 TSSOP | U28-3 | Sync Extractor |
| MAX9540EUI | 28 TSSOP | U28-3 | Sync Extractor |

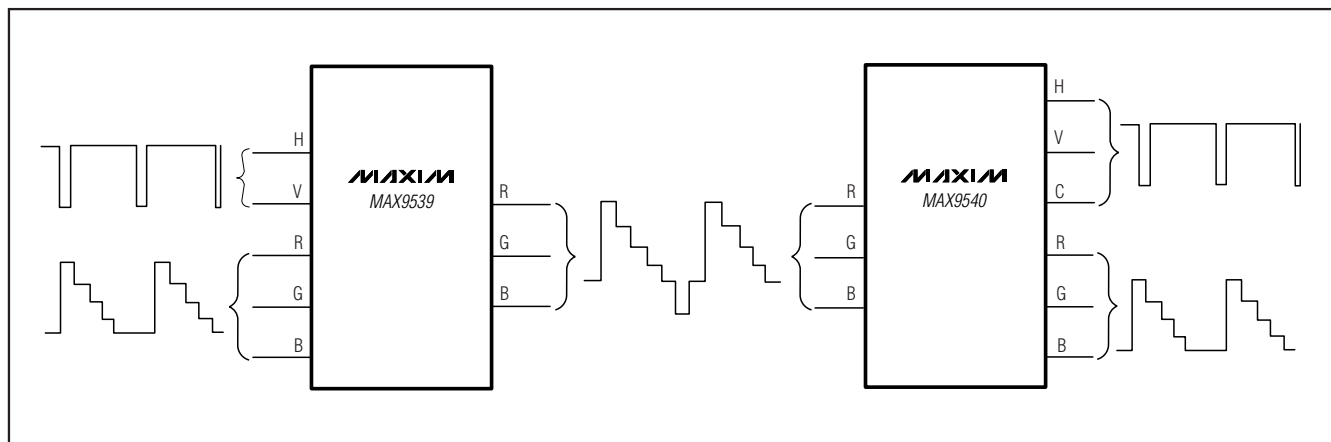
Note: All devices are specified over the -40°C to +85°C operating temperature range.

+Denotes lead-free package.

*Future product—contact factory for availability.

Pin Configurations appear at end of data sheet.

Chipset Diagram



Graphics Video Sync Adder/Extractor

ABSOLUTE MAXIMUM RATINGS

| | | |
|--|--|---|
| V _{CC} to GND | -0.3V to +6V | Continuous Power Dissipation (T _A = +70°C) 28-Pin TSSOP (U28-3) Single-Layer Board (derate 13mW/°C above +70°C) 1039mW 28-Pin TSSOP (U28-3) Multilayer Board (derate 14.3mW/°C above +70°C) 1143mW |
| V _{EE} to GND | -6V to +0.3V | |
| IN _R , IN _G , IN _B , REST _R , REST _G , REST _B | (V _{EE} - 0.3V) to (V _{CC} + 0.3V) | Operating Temperature -40°C to +85°C Junction Temperature +150°C Storage Temperature Range -65°C to +150°C Lead Temperature (soldering, 10s) +300°C |
| OUT _R , OUT _G , OUT _B Short Circuit to GND (Note 1) | Continuous | |
| OUT _R , OUT _G , OUT _B Short Circuit to V _{CC} |5s | |
| MAX9539: HSYNC, VSYNC, SP _H , SP _V | -0.3V to (V _{CC} + 0.3V) | |
| MAX9540: HSYNC, CSYNC, VSYNC Short Circuit to GND |Continuous | |
| HSYNC, CSYNC, VSYNC Short Circuit to V _{CC} |1min | |
| SP _C , SP _V , SP _H |-0.3V to (V _{CC} + 0.3V) | |

Note 1: Continuous power dissipation rating must also be observed.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

MAX9539 DC ELECTRICAL CHARACTERISTICS

(V_{CC} = +5V, V_{EE} = -5V, GND = 0V, R_L = 150Ω to GND, T_A = -40°C to +85°C, unless otherwise specified. Typical values are at T_A = +25°C.) (Notes 2 and 3)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--|---|---|-------|-------|-------|-------|
| Supply Voltage Range | V _{CC} | Guaranteed by PSRR test | 4.5 | | 5.5 | V |
| | V _{EE} | Guaranteed by PSRR test | -5.5 | | -4.5 | |
| Quiescent Supply Current | I _{CC} | R _L = ∞ | | 61 | 90 | mA |
| | I _{EE} | R _L = ∞ | | 55 | 75 | |
| Input Voltage Range | V _{IN} | Inferred from voltage gain test | 0 | | 1 | V |
| DC-Restore Input Voltage Range | ΔV _{IN_RESTORE} | Inferred from output DC-Restore Rejection Ratio test | -0.30 | | +0.30 | V |
| DC-Restore Rejection Ratio | DCRR (ΔV _{OS} / ΔV _{IN_RESTORE}) | V _{IN_RESTORE} = -0.3V to +0.3V | 28 | 50 | | dB |
| Input Bias Current | I _B | | | ±2 | ±30 | μA |
| Input Resistance | R _{IN} | | | 400 | | kΩ |
| Output Sync Amplitude | V _{SYNC} | H or V sync is active | -2.65 | -2.35 | -2.05 | V |
| Output Offset Voltage | V _{OS} | ΔV _{IN_RESTORE} = 0V, T _A = +25°C (Note 4) | | ±1 | ±8 | mV |
| Temperature Coefficient of Output Offset Voltage | TCV _{OS} (ΔV _{OS} / ΔT _A) | T _A = -40°C to +85°C | | -24 | | μV/°C |
| Voltage Gain | G | V _{IN} = 0 to +1V | +1.95 | +2 | +2.05 | V/V |
| Gain Matching | ΔG | R to G to B | | ±1 | ±2 | % |
| Gain Linearity | | | | 0.02 | | % |
| Power-Supply Rejection Ratio | PSRR ΔV _{OS} / Δ(V _{CC} - V _{EE}) | V _{CC} , V _{EE} = ±4.5V to ±5.5V | 50 | 70 | | dB |

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MAX9539 DC ELECTRICAL CHARACTERISTICS (continued)

($V_{CC} = +5V$, $V_{EE} = -5V$, $GND = 0V$, $R_L = 150\Omega$ to GND , $T_A = -40^\circ C$ to $+85^\circ C$, unless otherwise specified. Typical values are at $T_A = +25^\circ C$.) (Notes 2 and 3)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--------------------------------------|-------------|------------|-----|---------|-----|---------|
| HSYNC, VSYNC INPUTS | | | | | | |
| High Input Voltage | V_{IH} | | 2 | | | V |
| Low Input Voltage | V_{IL} | | | | 0.8 | V |
| High Input Current | I_{IH} | $V_I = 5V$ | | 10 | 60 | μA |
| Low Input Current | I_{IL} | $V_I = 0V$ | | 2.5 | | μA |
| SP_H, SP_V INPUTS | | | | | | |
| High Input Voltage | V_{IH} | | 2 | | | V |
| Low Input Voltage | V_{IL} | | | | 0.8 | V |
| High Input Current | I_{IH} | $V_I = 5V$ | | 0.1 | 20 | μA |
| Low Input Current | I_{IL} | $V_I = 0V$ | | 1 | 20 | μA |
| REST_R, REST_B, REST_G INPUTS | | | | | | |
| Hold-Mode Droop Current | I_{DROOP} | | | ± 2 | | nA |

MAX9539 AC ELECTRICAL CHARACTERISTICS

($V_{CC} = +5V$, $V_{EE} = -5V$, $GND = 0V$, $R_L = 150\Omega$ to GND , $T_A = -40^\circ C$ to $+85^\circ C$, unless otherwise specified. Typical values are at $T_A = +25^\circ C$.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|-------------------------------------|---------------|-------------------------------|-----|-----------|-----|-----------------|
| Large-Signal Bandwidth | LSBW | $V_{OUT} = 2V_{P-P}$ | | 180 | | MHz |
| Slew Rate | SR | $V_{OUT} = 2V_{P-P}$ | | 900 | | V/ μs |
| Channel-to-Channel Crosstalk | X_{TALK} | $V_{OUT} = 2V_{P-P}$ at 10MHz | | -60 | | dB |
| Settling Time | t_S | $V_{OUT} = 2V_{P-P}$ to 0.1% | | 15 | | ns |
| Input Voltage-Noise Density | e_n | $f = 100kHz$ | | 30 | | nV/ \sqrt{Hz} |
| Input Current-Noise Density | i_n | $f = 100kHz$ | | 12 | | pA/ \sqrt{Hz} |
| Sync Timing Delay | t_D | H sync only (Note 5) | | -20 | | ns |
| Channel-to-Channel Sync Timing Skew | $\Delta(t_D)$ | H sync only (Note 5) | | 1 | | ns |
| Sync Edge Jitter | t_{JITTER} | | | 200 | | pSP-P |
| Line Droop | | $f = 50kHz$ | | 0.01 | | % |
| Field Tilt | | $f = 60Hz$ | | 0.04 | | % |
| Sync Frequency Range | f_H | H sync | | 15 to 150 | | kHz |
| | f_V | V sync | | 40 to 100 | | Hz |

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MAX9540 DC ELECTRICAL CHARACTERISTICS

($V_{CC} = +5V$, $V_{EE} = -5V$, $GND = 0V$, $R_L = 150\Omega$ to GND , $T_A = -40^\circ C$ to $+85^\circ C$, unless otherwise specified. Typical values are at $T_A = +25^\circ C$.) (Notes 2 and 3)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--|---|--|-------|---------|----------|------------------|
| Supply Voltage Range | V_{CC} | Guaranteed by PSRR test | 4.5 | | 5.5 | V |
| | V_{EE} | Guaranteed by PSRR test | -5.5 | | -4.5 | |
| Quiescent Supply Current | I_{CC} | $R_L = \infty$ | | 61 | 90 | mA |
| | I_{EE} | $R_L = \infty$ | | 54 | 75 | |
| Input Voltage Range | V_{IN} | Inferred from voltage gain test | 0 | | 1 | V |
| DC-Restore Input Voltage Range | $\Delta V_{IN_RESTORE}$ | Inferred from DC-Restore Rejection Ratio test | -0.30 | | +0.30 | V |
| DC-Restore Rejection Ratio | $\frac{DCRR}{(\Delta V_{OS} / \Delta V_{IN_RESTORE})}$ | $V_{IN_RESTORE} = -0.3V$ to $+0.3V$ | 28 | 50 | | dB |
| Input Bias Current | I_B | | | ± 2 | ± 30 | μA |
| Input Resistance | R_{IN} | | | 400 | | $k\Omega$ |
| Output Black Level | V_{BLACK} | H or V sync is active: $V_{IN} < -1V$ | | ± 1 | ± 16 | mV |
| Output Offset Voltage | V_{OS} | $\Delta V_{IN_RESTORE} = 0V$, $T_A = +25^\circ C$ (Note 4) | | ± 1 | ± 8 | mV |
| Temperature Coefficient of Output Offset Voltage | $\frac{TCV_{OS}}{(\Delta V_{OS} / \Delta T_A)}$ | $T_A = -40^\circ C$ to $+85^\circ C$ | | -24 | | $\mu V/^\circ C$ |
| Voltage Gain | G | $V_{IN} = 0$ to $+1V$ | +1.95 | +2 | +2.05 | V/V |
| Gain Matching | ΔG | R to G to B | | ± 1 | ± 2 | % |
| Gain Linearity | | | | 0.02 | | % |
| Power-Supply Rejection Ratio | $\frac{PSRR}{\Delta V_{OS} / \Delta(V_{CC} - V_{EE})}$ | $V_{CC}, V_{EE} = \pm 4.5V$ to $\pm 5.5V$ | 50 | 70 | | dB |
| SP_H, SP_V, SP_C INPUTS | | | | | | |
| High Input Voltage | V_{IH} | | 2 | | | V |
| Low Input Voltage | V_{IL} | | | | 0.8 | V |
| High Input Current | I_{IH} | $V_I = 5V$ | | 0.01 | 20 | μA |
| Low Input Current | I_{IL} | $V_I = 0V$ | | 1 | 20 | μA |
| REST_R, REST_G, REST_B INPUTS | | | | | | |
| Hold-Mode Droop Current | I_{DROOP} | | | ± 2 | | nA |
| HSYNC, VSYNC, CSYNC OUTPUTS | | | | | | |
| High Voltage Level | V_{OH} | $I_{OH}(\text{source}) = +8mA$ | 2.4 | | | V |
| Low Voltage Level | V_{OL} | $I_{OL}(\text{sink}) = -8mA$ | | | 0.5 | V |

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MAX9540 AC ELECTRICAL CHARACTERISTICS

($V_{CC} = +5V$, $V_{EE} = -5V$, $GND = 0V$, $R_L = 150\Omega$ to GND , $T_A = -40^\circ C$ to $+85^\circ C$, unless otherwise specified. Typical values are at $T_A = +25^\circ C$.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|------------------------------|---------------|-------------------------------|-----|-----------|-----|-----------------|
| Large-Signal Bandwidth | LSBW | $V_{OUT} = 2V_{P-P}$ | | 180 | | MHz |
| Slew Rate | SR | $V_{OUT} = 2V_{P-P}$ | | 900 | | V/ μs |
| Channel-to-Channel Crosstalk | XTALK | $V_{OUT} = 2V_{P-P}$ at 10MHz | | -60 | | dB |
| Settling Time | t_S | $V_{OUT} = 2V_{P-P}$ to 0.1% | | 15 | | ns |
| Input Voltage-Noise Density | e_n | $f = 100kHz$ | | 30 | | nV/ \sqrt{Hz} |
| Input Current-Noise Density | i_n | $f = 100kHz$ | | 12 | | pA/ \sqrt{Hz} |
| Sync Timing Delay | t_D | H sync only (Note 5) | | -10 | | ns |
| Sync Timing Skew | $\Delta(t_D)$ | H sync only (Note 5) | | 1 | | ns |
| Sync Edge Jitter | t_{JITTER} | | | 200 | | psp-p |
| Line Droop | | $f = 50kHz$ | | 0.01 | | % |
| Field Tilt | | $f = 60Hz$ | | 0.04 | | % |
| Sync Frequency Range | f_H | H sync | | 15 to 150 | | kHz |
| | f_V | V sync | | 40 to 100 | | Hz |

Note 2: All devices are 100% production tested at $T_A = +25^\circ C$. Specifications over temperature limits are guaranteed by design.

Note 3: DC restore is not active. HSYNC and VSYNC are not applied. REST_R, REST_G, and REST_B are grounded.

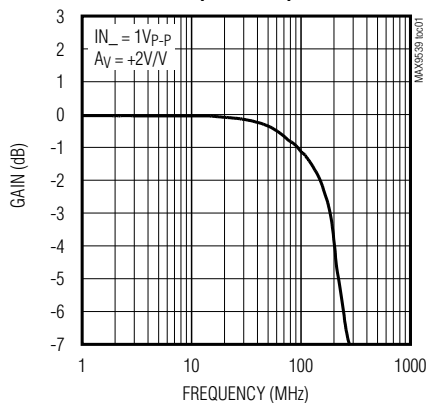
Note 4: DC restore is active. REST_R, REST_G, and REST_B are bypassed with 1nF to ground.

Note 5: The sync timing error is measured as follows: The input signals are measured from the falling edge of H sync/V sync to the start of active video, called t_1 . The output signal is then measured from the falling edge of H sync/V sync to the start of active video, called t_2 . All measurements are at the 50% points as shown in Figure 1.

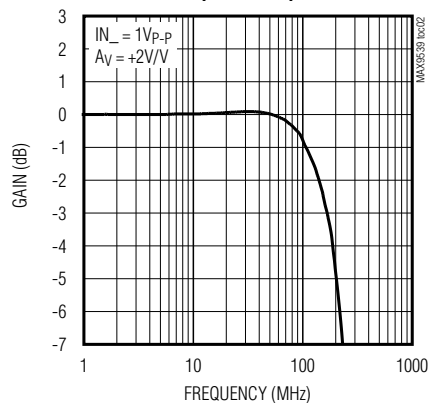
Typical Operating Characteristics

($T_A = +25^\circ C$, $V_{CC} = +5V$, $V_{EE} = -5V$, $GND = 0V$, $R_L = 150\Omega$ to GND , unless otherwise noted.)

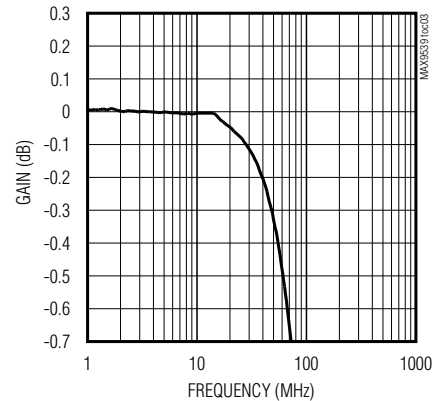
LARGE-SIGNAL FREQUENCY RESPONSE (MAX9539)



LARGE-SIGNAL FREQUENCY RESPONSE (MAX9540)



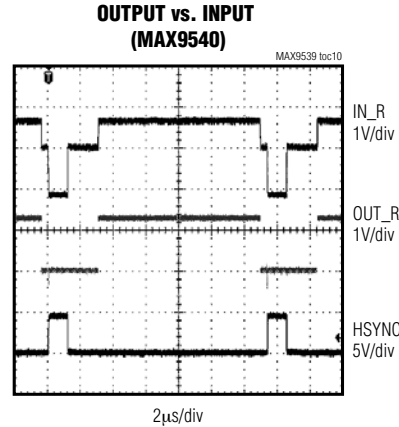
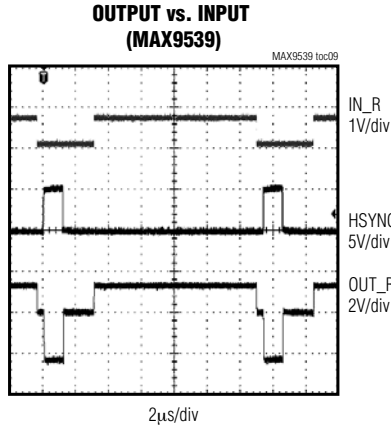
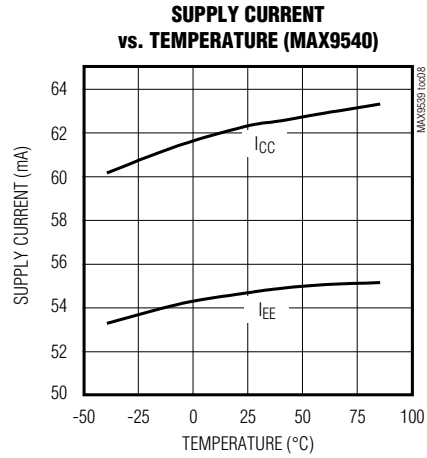
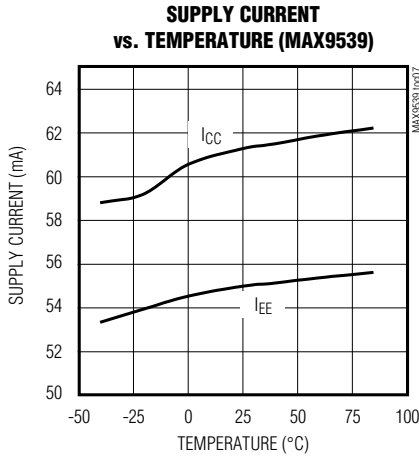
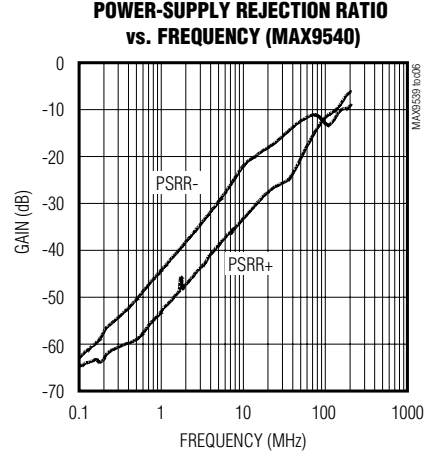
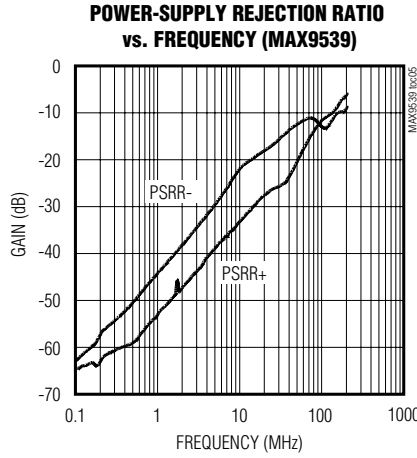
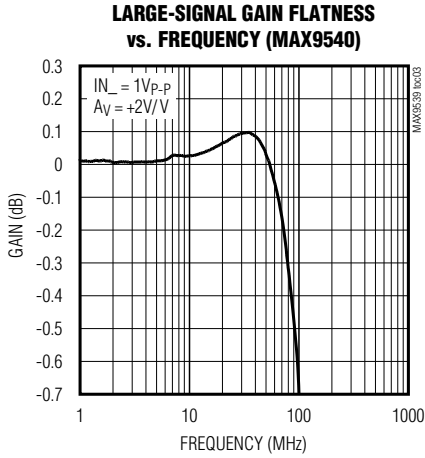
LARGE-SIGNAL GAIN FLATNESS vs. FREQUENCY (MAX9539)



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Typical Operating Characteristics (continued)

($T_A = +25^\circ\text{C}$, $V_{CC} = +5\text{V}$, $V_{EE} = -5\text{V}$, $\text{GND} = 0\text{V}$, $R_L = 150\Omega$ to GND , unless otherwise noted.)



Graphics Video Sync Adder/Extractor

MAX9539 Pin Description

| PIN | NAME | FUNCTION |
|--|--------|--|
| 1 | IN_R | Red Video Input |
| 2, 7, 12 | GND | Ground |
| 3 | REST_R | Red DC Restore. Connect a 1nF capacitor from REST_R to GND. |
| 4, 9, 10, 14, 15, 20, 21, 22, 25 | N.C. | No Connection. Not internally connected. |
| 5 | I.C. | Internally Connected. For best performance, connect this pin to GND. |
| 6 | IN_G | Green Video Input |
| 8 | REST_G | Green DC Restore. Connect a 1nF capacitor from REST_G to GND. |
| 11 | IN_B | Blue Video Input |
| 13 | REST_B | Blue DC Restore. Connect a 1nF capacitor from REST_B to GND. |
| 16 | VSYNC | Vertical Sync Input |
| 17 | SP_V | Vertical Sync Polarity Input |
| 18 | OUT_B | Blue Output with Vertical Sync |
| 19 | VEE | Negative Power-Supply Input. Bypass with a 0.1 μ F capacitor to GND. |
| 23 | OUT_G | Green Output with Composite Sync. |
| 24 | VCC | Positive Power-Supply Input. Bypass with a 0.1 μ F capacitor to GND. |
| 26 | HSYNC | Horizontal Sync Input |
| 27 | SP_H | Horizontal Sync Polarity Input |
| 28 | OUT_R | Red Output with Horizontal Sync |

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MAX9540 Pin Description

| PIN | NAME | FUNCTION |
|--------------------------|--------|--|
| 1 | IN_R | Red Video Input with Horizontal Sync |
| 2, 7, 12 | GND | Ground |
| 3 | REST_R | Red DC Restore. Connect a 1nF capacitor from REST_R to GND. |
| 4, 9, 10, 14, 15, 20, 25 | N.C. | No Connection. Not internally connected. |
| 5 | I.C. | Internally Connected. For best performance, connect this pin to GND. |
| 6 | IN_G | Green Video Input with Composite Sync |
| 8 | REST_G | Green DC Restore. Connect a 1nF capacitor from REST_G to GND. |
| 11 | IN_B | Blue Video Input with Vertical Sync |
| 13 | REST_B | Blue DC Restore. Connect a 1nF capacitor from REST_B to GND. |
| 16 | VSYNC | Vertical Sync Output |
| 17 | SP_V | Vertical Sync Polarity Input |
| 18 | OUT_B | Blue Video Output |
| 19 | VEE | Negative Power-Supply Input. Bypass with a 0.1 μ F capacitor to GND. |
| 21 | CSYNC | Composite Sync Output |
| 22 | SP_C | Composite Sync Polarity Input |
| 23 | OUT_G | Green Video Output |
| 24 | VCC | Positive Power-Supply Input. Bypass with a 0.1 μ F capacitor to GND. |
| 26 | HSYNC | Horizontal Sync Output |
| 27 | SP_H | Horizontal Sync Polarity Input |
| 28 | OUT_R | Red Video Output |

Detailed Description

The MAX9539/MAX9540 chipset provides a 3-wire (RGB) interface for 5-wire (RGBHV) video by adding and extracting the H, V, and composite sync from the graphics video signals. This chipset eliminates the problem of sync-to-video timing (skew errors) in a 5-wire interface, while reducing the number of channels required when transporting video signals.

The MAX9539 mixes the H and V sync signals and adds them to create a 3-wire interface from a 5-wire (RGBHV) input. The MAX9540 recovers the H and V sync signals to create a 5-wire (RGBHV) interface from the 3-wire input. The MAX9540 also provides a composite sync output.

The chipset includes the MAX9539 sync adder and the MAX9540 sync extractor with 180MHz large-signal bandwidths to address display resolutions up to 1600 x 1200 at 85Hz for VGA-to-UXGA applications. Both devices feature a DC-restore function, which virtually eliminates any changes in black level. The chipset uses a proprietary H and V sync addition/extraction scheme (true sync) to minimize skew errors.

MAX9539 Sync Adder

The MAX9539 mixes the H and V sync signals and adds them to create a 3-wire interface from a 5-wire (RGBHV) input. Sync signals are added to the input video signals. Horizontal sync is added to red video, vertical sync is added to blue video, and composite sync is added to green video. Composite sync is the XOR function between H sync and V sync and is internally generated by the MAX9539. The sync level of the video outputs is -2.4V. The DC-restore function removes any DC offset ($\Delta V_{IN_RESTORE}$) in the RGB video inputs and sets the output black level to 0V at the back porch of the H sync. Therefore, the output black level is set to 0V at the beginning of every line.

Figure 2 illustrates the functionality of the MAX9539. In this example, the sync signals are of positive polarity.

MAX9540 Sync Extractor

The MAX9540 recovers the H and V sync signals to create a 5-wire (RGBHV) interface from the 3-wire input. The output video signals are obtained by removing the sync pulses of the input video. The sync outputs correspond to the sync pulses of the input video: horizontal sync is

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obtained from the red input, vertical sync is obtained from the blue input, and composite sync is obtained from the green input. Like the MAX9539, the DC-restore function removes any DC offset in the RGB video inputs and sets the output black levels to 0V. This happens at the back porch (trailing edge) of the sync pulse.

Figure 3 illustrates the functionality of the MAX9540. In this example, the sync signals are of positive polarity.

DC Restore

The MAX9539/MAX9540 DC-restore function removes the input signal DC level and restores 0V for the black level of the output video signal. 1nF restore capacitors are needed for the sample-and-hold circuitry at REST_R, REST_G, and REST_B. A value less than 0.5nF can cause AC instability in the sample-and-hold circuitry. A value higher than 2nF increases the settling time of the sample-and-hold circuitry, shifting the output black level from 0V.

Sync Polarity

Sync polarity refers to the idle state and pulse amplitude of the sync pulse. A sync pulse that idles low and pulses high is referred to as a positive sync pulse. A sync pulse that idles high and pulses low is referred to as a negative sync pulse as seen in Figure 4. To accommodate positive and negative sync input signals, the MAX9539/MAX9540 have vertical and horizontal sync polarity inputs (SP_V and SP_H). Drive SP_V or SP_H high for positive sync polarity. Drive SP_V or SP_H low for negative sync polarity. The MAX9540 also has a composite polarity input (SP_C). Drive SP_C high for positive sync polarity or drive SP_C low for negative sync polarity (Table 1).

Layout and Power-Supply Bypassing

The MAX9539/MAX9540 have an extremely high bandwidth and require careful board layout. For best performance use constant-impedance microstrip or stripline techniques.

To realize the full AC performance of these high-speed amplifiers, pay careful attention to power-supply bypassing and board layout. The PC board should have at least two layers: a signal and power layer on one side, and a large, low-impedance ground plane on the other side. The ground plane should be as free of voids as possible. With multilayer boards, locate the ground plane on a layer that incorporates no signal or power traces.

Observe the following guidelines when designing the board regardless of whether or not a constant-impedance board is used.

- 1) Do not use wire-wrap boards or breadboards.

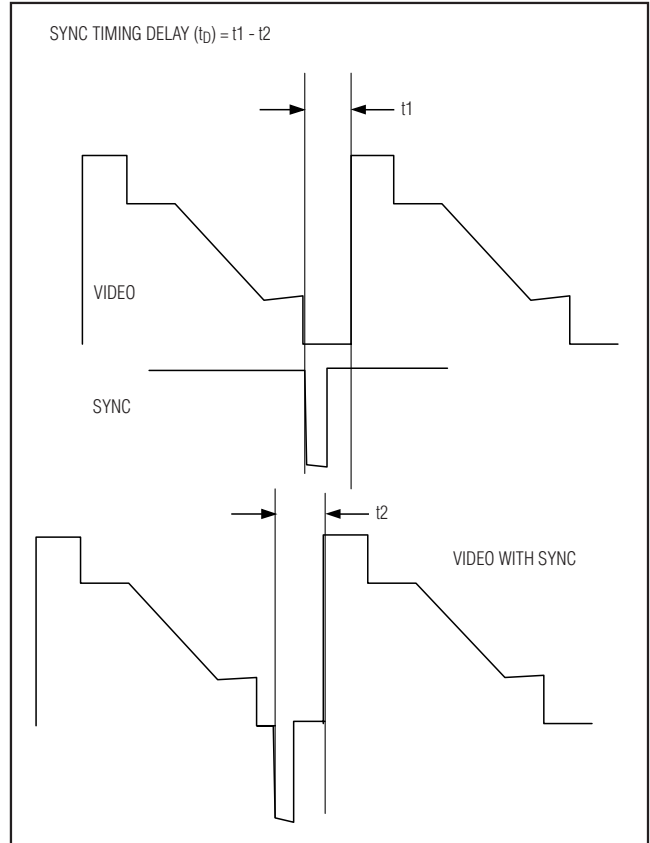


Figure 1. Sync Timing Delay (t_D) = t₁ - t₂

Table 1. Sync Polarity Table

| INPUT LOGIC VALUE | SP_V | SP_H | SP_C (MAX9540) |
|-------------------|---------------|---------------|----------------|
| 1 | Positive sync | Positive sync | Positive sync |
| 0 | Negative sync | Negative sync | Negative sync |

- 2) Do not use IC sockets; they increase parasitic capacitance and inductance.
- 3) Keep lines as short and as straight as possible. Do not make 90° turns; round all corners.
- 4) Observe high-frequency bypassing techniques to maintain the amplifier's accuracy and stability.
- 5) Use surface-mount components. They generally have shorter bodies and lower parasitic reactance, yielding better high-frequency performance than through-hole components.

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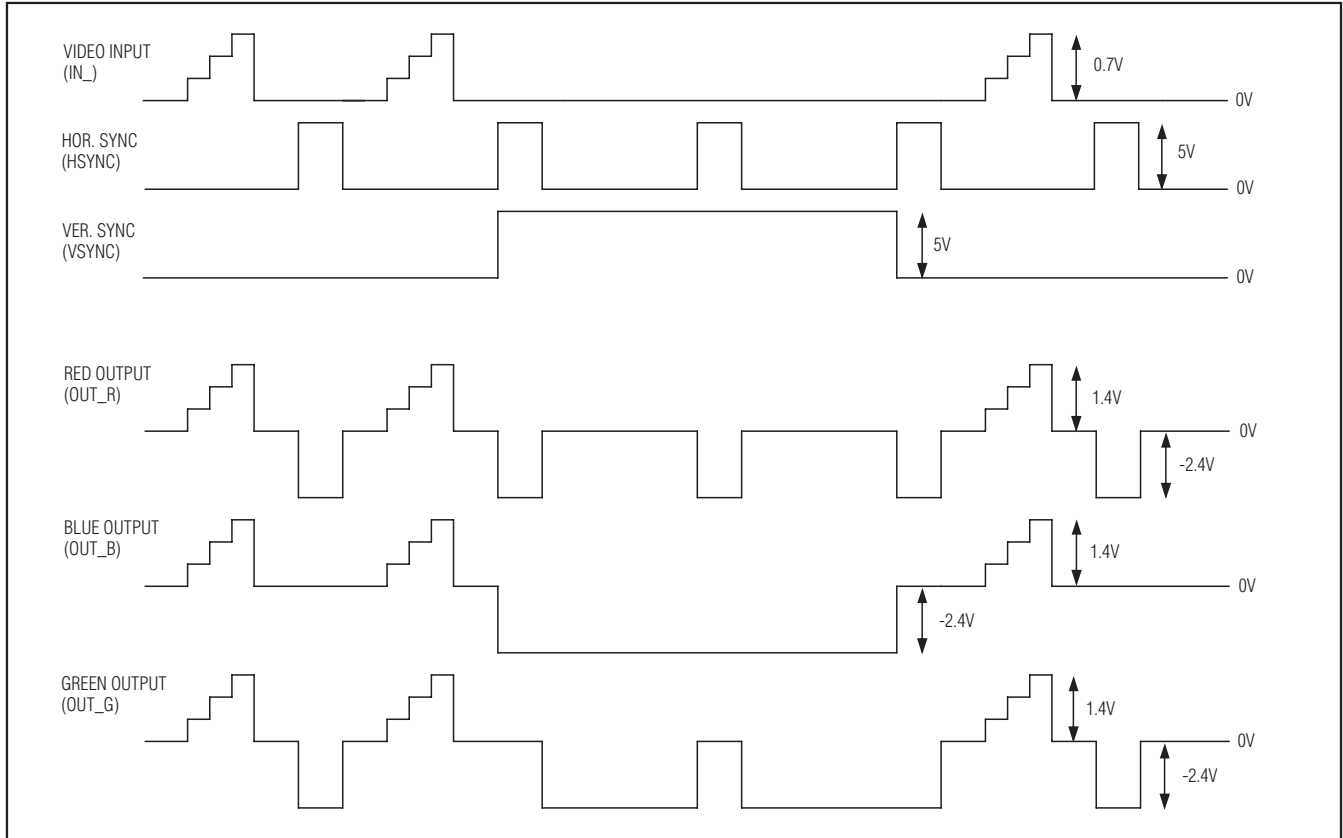


Figure 2. MAX9539 Input and Output Functionality

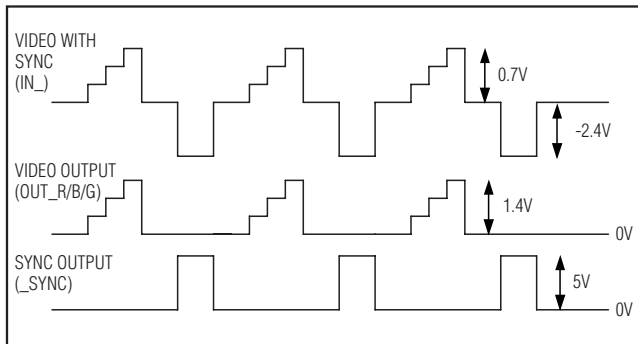


Figure 3. MAX9540 Input and Output Functionality

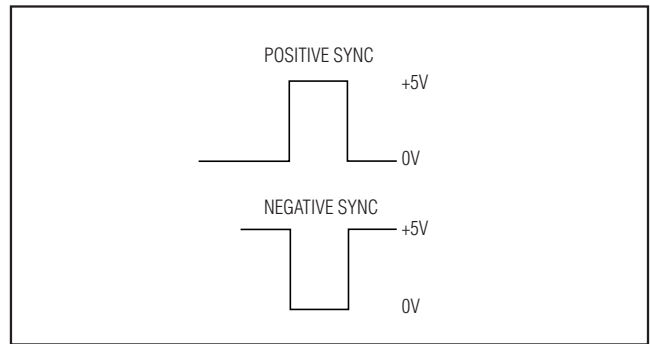


Figure 4. Sync Pulse Polarity

The bypass capacitors should include a 0.1µF ceramic surface-mount capacitor between each supply pin and the ground plane, located as close to the package as possible. Optionally, place a 10µF tantalum capacitor at the power-supply pins' points of entry to the PC board to ensure the integrity of incoming supplies. The power-supply trace should lead directly from the tanta-

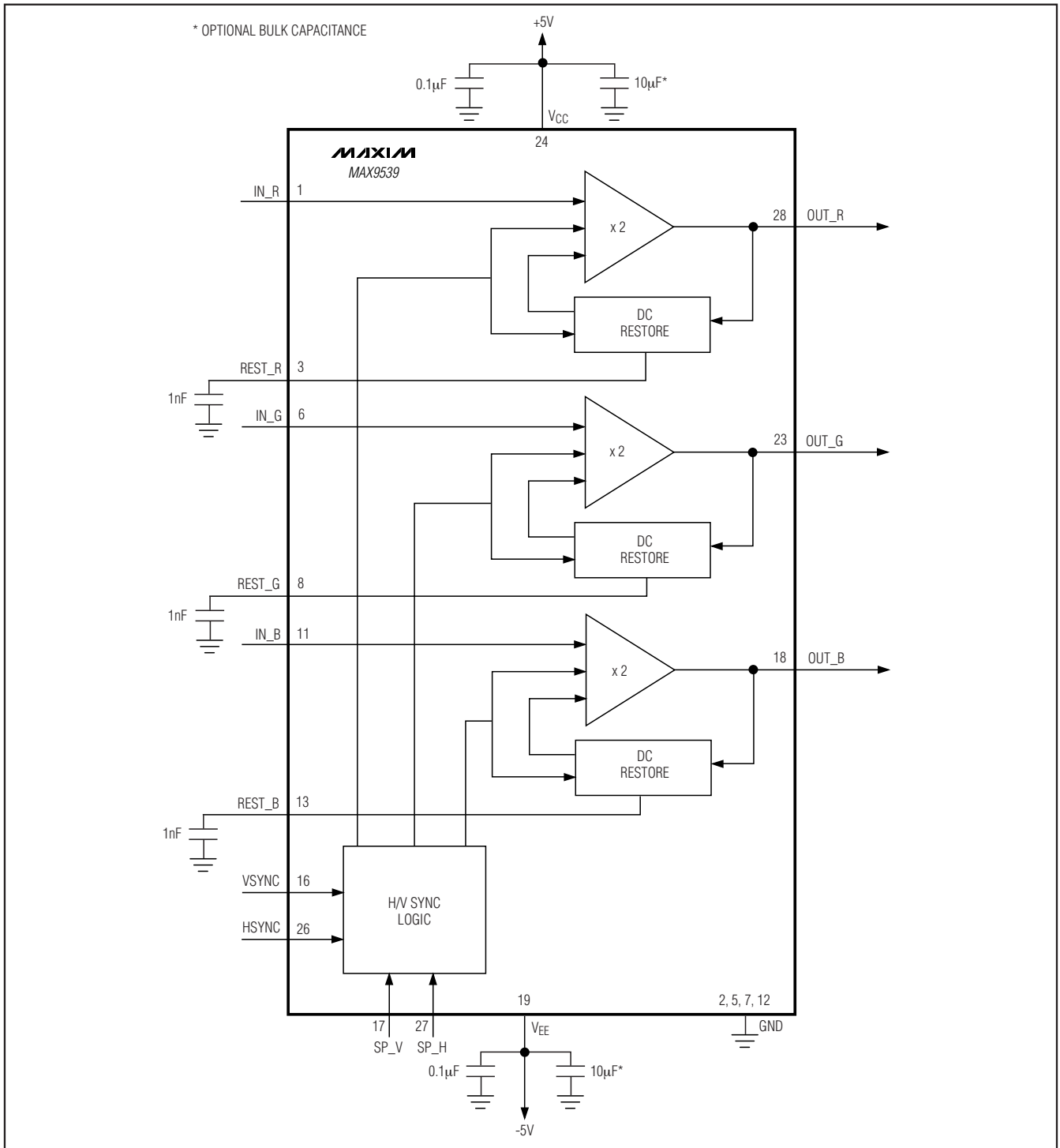
lum capacitor to the VCC and VEE pins. To minimize parasitic inductance, keep PC traces short and use surface-mount components.

Use surface-mount resistors for input termination and output back termination. Place the termination resistors as close to the IC as possible.

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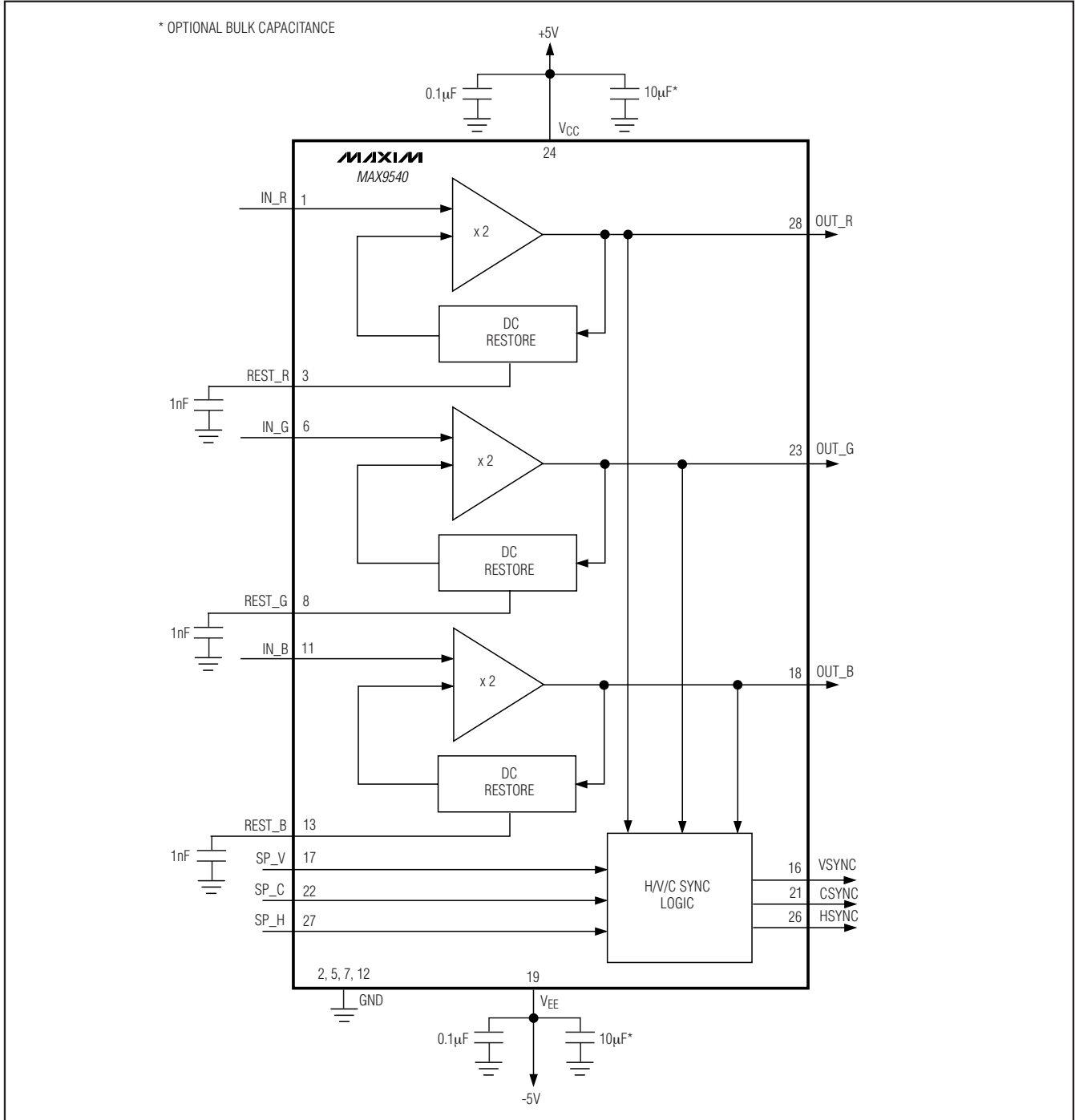
Functional Diagrams

MAX9539/MAX9540



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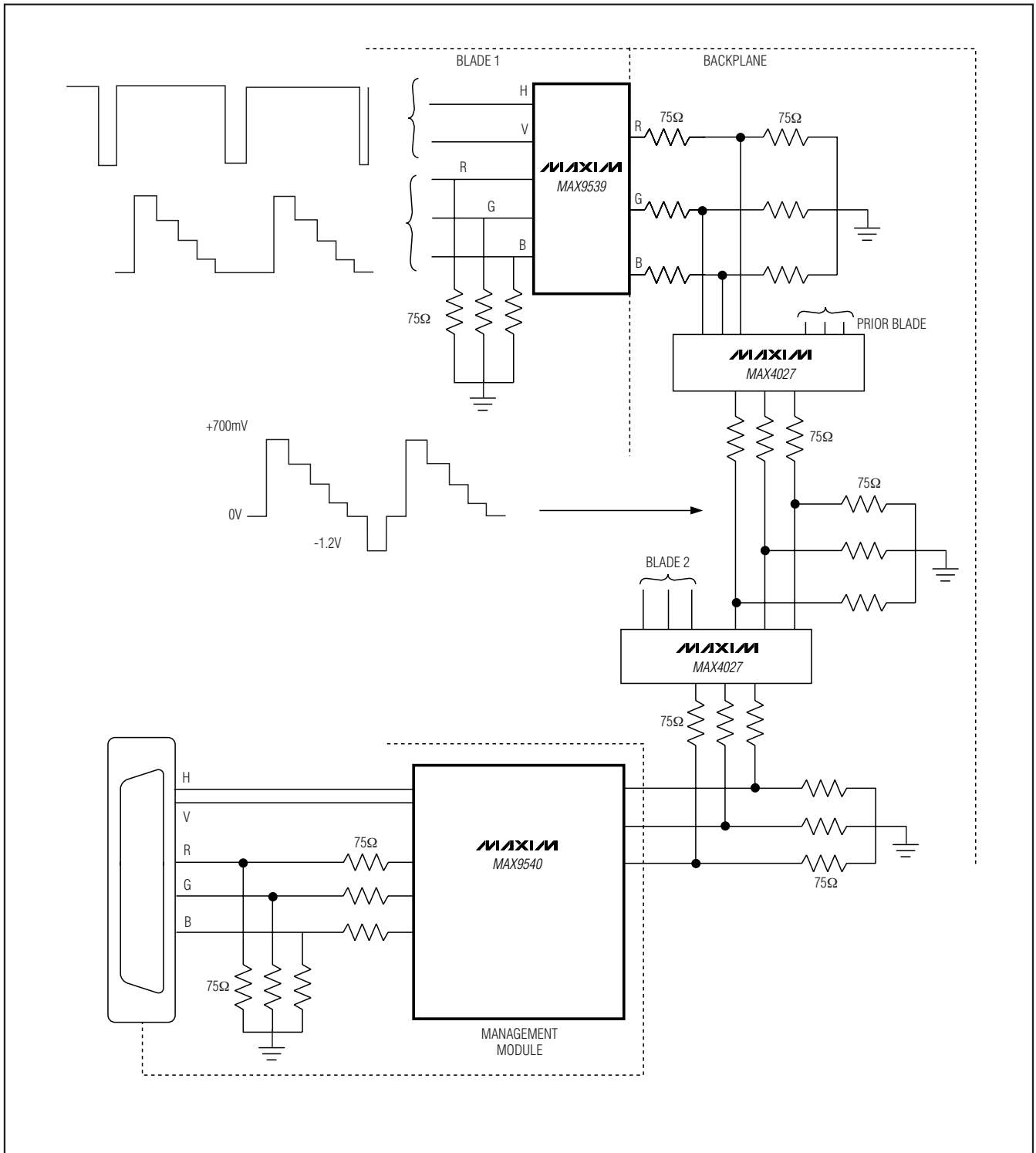
Functional Diagrams (continued)



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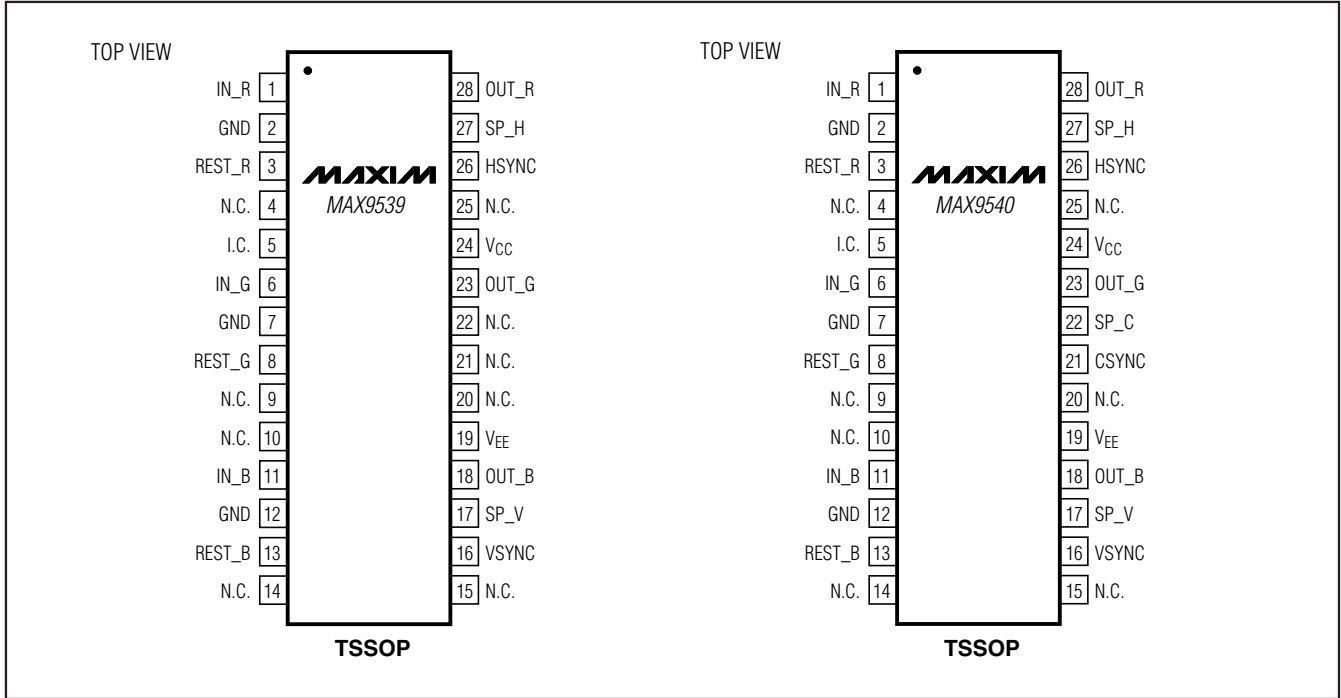
Typical Application Diagram

MAX9539/MAX9540



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Pin Configurations



Chip Information

PROCESS: Bipolar

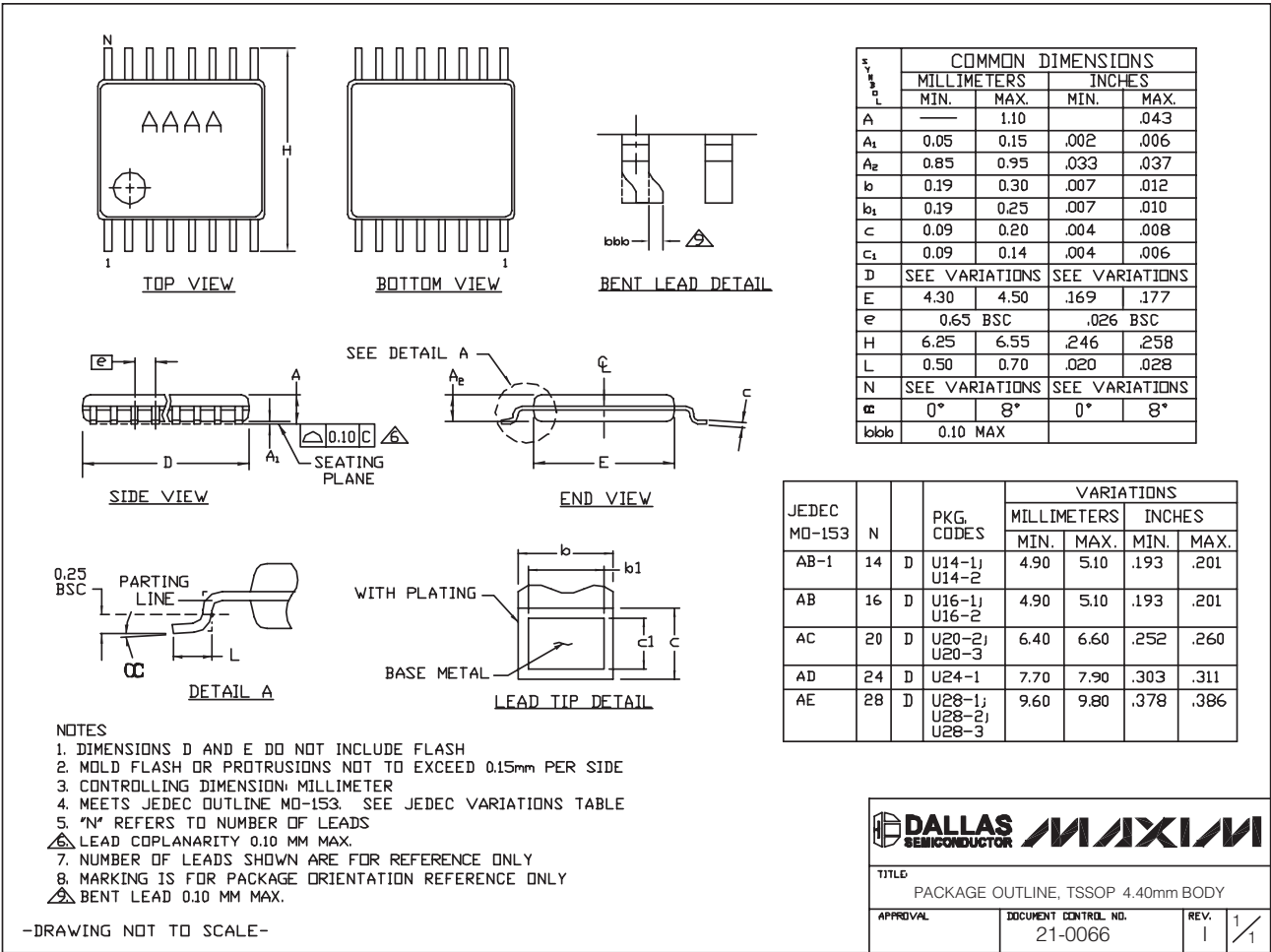
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Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to www.maxim-ic.com/packages.)

MAX9539/MAX9540

TSSOP4.40mm.EPS



Revision History

Pages changed at Rev 2: 1, 2, 4, 15

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