3.3V, 5-differential Channel LVDS Switch Targeted for 24bit Displays

Features

- Designed specifically to switch LVDS signals
- V_{DD} = 3.3V +/-10%
- ESD tolerance on video I/O pins is up to 12kV HBM
- -3dB BW of 870MHz (typ)
- Low Xtalk, (-28dB typ)
- Low and Flat ON-STATE resistance (Ron = 3ohm, Ron(Flat) = 0.5ohm, typ)
- Low input/output capacitance (Con = 6pF, typ)
- Packaging (Pb-free and Green):
  − 56 contact TQFN (ZFE)
  − 42 contact TQFN (ZHE)

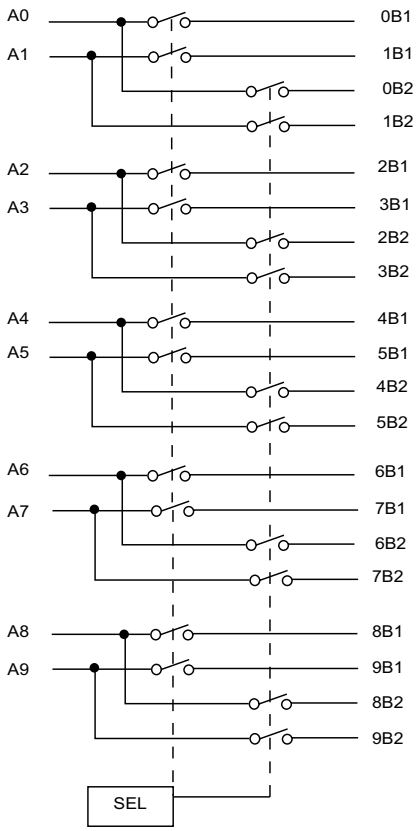
Applications

- Routes physical layer signals for high bandwidth

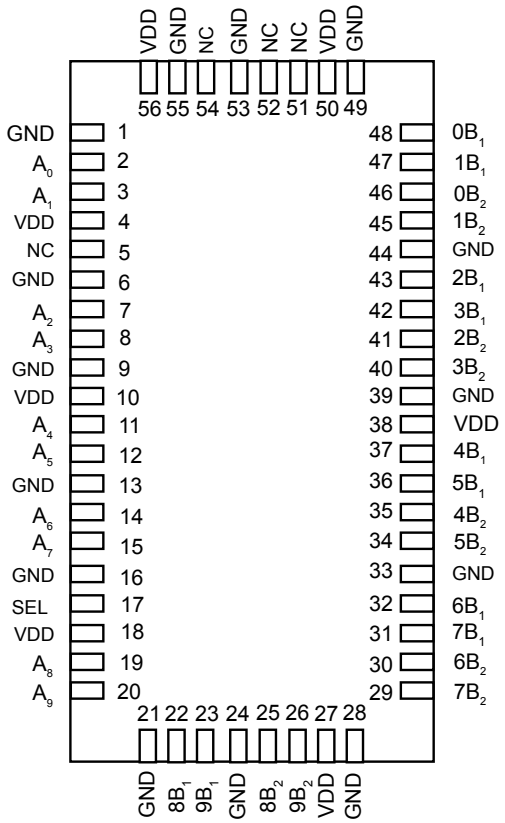
Description

Pericom's PI3LVD512 is a 5-differential channel LVDS mux/demux used to switch between multiple LVDS sources or end points. In a notebook application where analog video signals are found in both the notebook and the dock, a switch solution is required to switch between the two video port locations. With the high bandwidth of 870MHz, the signal integrity will remain strong even through the long FR4 trace between the notebook and the docking station. In addition to high signal performance, the video signals are also protected against high ESD with integrated diodes to V_{DD} and GND that will support up to 12kV of ESD HBM protection.

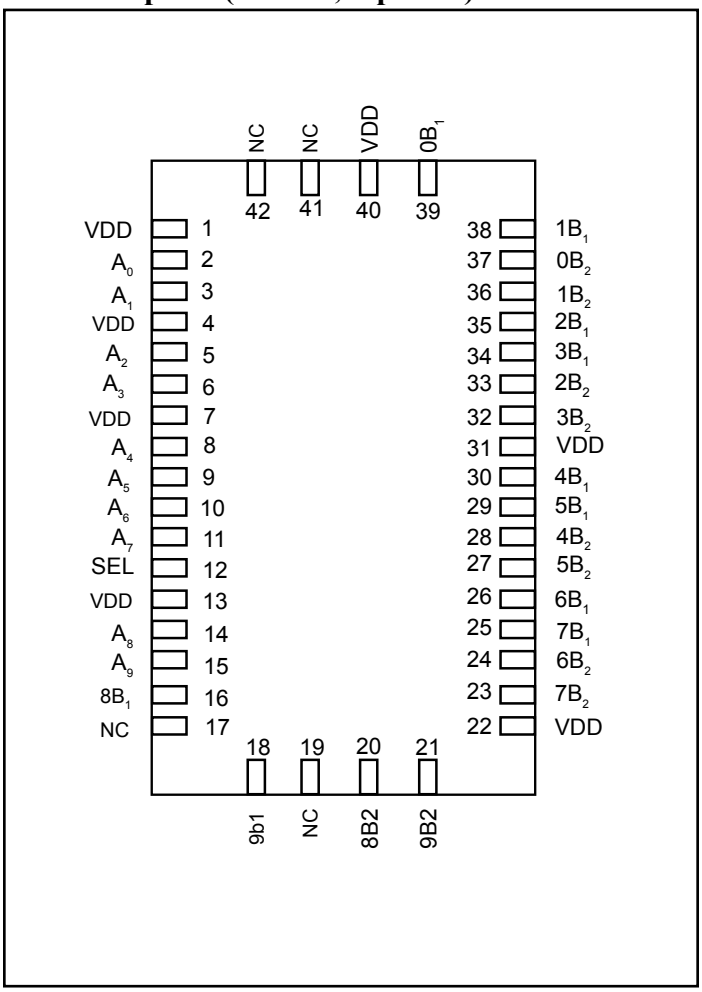
Block Diagram



Pin Description (56ZFE, top view)



Pin Description (42ZHE, top view)



Maximum Ratings

(Above which useful life may be impaired. For user guidelines, not tested.)

Storage Temperature.....–65°C to +150°C
Supply Voltage to Ground Potential.....–0.5V to +4.0V
DC Input Voltage.....–0.5V to +5.5V
DC Output Current.....120mA
Power Dissipation.....0.5W

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Truth Table

Input SEL	Input/Output An	Function	
L	nB_1	$A_n = nB_1$	nB_2 high impedance mode
H	nB_2	$A_n = nB_2$	nB_1 high impedance mode

DC Electrical Characteristics for Video Switching over Operating Range

(T_A = –40°C to +85°C, V_{DD} = 3.3V ±10%)

Paramenter	Description	Test Conditions(1)	Min.	Typ.(2)	Max.	Units
V_{IH}	Input HIGH Voltage	Guaranteed HIGH level	2	-	-	V
V_{IL}	Input LOW Voltage	Guaranteed LOW level	–0.5	-	0.8	
V_{IK}	Clamp Diode Voltage	V_{DD} = Max., I_{SEL} = –18mA	-	–0.7	–1.2	
I_{IH}	Input HIGH Current	V_{DD} = Max., V_{SEL} = V_{DD}	-	-	±5	µA
I_{IL}	Input LOW Current	V_{DD} = Max., V_{SEL} = GND	-	-	±5	
I_{OFF}	Power Down Leakage Current	V_{DD} = 0V, $V_A \le 3.6$	-	-	±5	
R_{ON}	Switch On-Resistance(3)	V_{DD} = Min., 0.9V ≤ V_{input} ≤ 1.6V, I_{input} = –40mA	-	2.8	3.5	Ω
$R_{FLAT(ON)}$	On-Resistance Flatness(4)	V_{DD} = Min., V_{input} @ 0V and 1.5V, I_{input} = –40mA	-	0.5	-	
ΔR_{ON}	On-Resistance match from center ports to any other port(4)	V_{DD} = Min., 0.9V ≤ V_{input} ≤ 1.6V, I_{input} = –40mA	-	0.9	2	

Capacitance (T_A = 25°C, f = 1MHz)

Parameters[4]	Description	Test Conditions[1]	Typ.[2]	Units
C_{IN}	Input Capacitance	V_{SEL} = 0V	2.7	pF
C_{OFF}	Port A/B Capacitance, Switch OFF		2	
C_{ON}	Switch Capacitance, Switch ON		6	

Notes:
1. For max. or min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{DD} = 3.3V, T_A = 25°C ambient and maximum loading.
3. Measured by the voltage drop between A and B pins at indicated current through the switch. On-Resistance is determined by the lower of the voltages on the two (A & B) pins.
4. This parameter is determined by device characterization but is not production tested.

Power Supply Characteristics

Parameters	Description	Test Conditions[1]	Min.	Typ.[2]	Max.	Units
I_{CC}	Quiescent Power Supply Current	V_{DD} = Max., V_{SEL} = GND or V_{DD}	-	-	500	µA

Notes:
1. For max. or min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{DD} = 3.3V, T_A = 25°C ambient and maximum loading.

Dynamic Electrical Characteristics Over the Operating Range (T_A=-40º to +85ºC, V_{DD}=3.3V±10%, GND=0V)

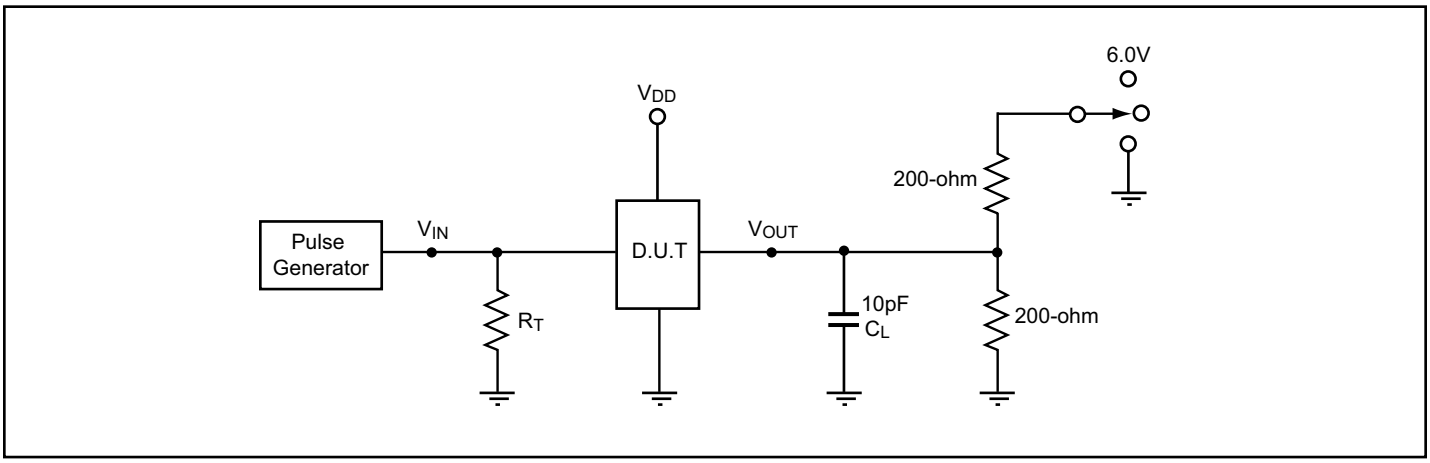
Parameter	Description	Test Conditions	Min.	Typ.[2]	Max.	Units
X_{TALK}	Crosstalk	f = 250MHz, See Fig. 2	-	-28	-	dB
O_{IRR}	OFF Isolation	f = 250MHz, See Fig. 3	-	-41	-	
BW	Bandwidth –3dB	See Fig. 1	-	880	-	MHz

Switching Characteristics

Paramenter	Description	Min.	Typ.[2]	Max.	Units
t_{PD}	Propagation Delay[2,3]	-	0.25		ns
t_{PZH}, t_{PZL}	Line Enable Time - SEL to Input, Output	0.5	-	15	
t_{PHZ}, t_{PLZ}	Line Disable Time - SEL to Input, Output	0.5	-	9	
$t_{b\text{-}b}$ (2)	Differential Bit-to-bit Skew	-	-	15	ps
$t_{ch\text{-}ch}$ (2)	Differential channel to channel skew	-	-	60	

Notes:
1. For max. or min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Guaranteed by design.
3. The switch contributes no propagational delay other than the RC delay of the On-Resistance of the switch and the load capacitance. The time constant for the switch alone is of the order of 0.25ns for 10pF load. Since this time constant is much smaller than the rise/fall times of typical driving signals, it adds very little propagational delay to the system. Propagational delay of the bus switch when used in a system is determined by the driving circuit on the driving side of the switch and its interactions with the load on the driven side.

Test Circuit for Electrical Characteristics(1)



Notes:
1. C_L = Load capacitance: includes jig and probe capacitance.
2. R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator
3. All input impulses are supplied by generators having the following characteristics: f = 10 MHz, $Z_O = 50\Omega$, $t_R \leq 2.5$ns, $t_F \leq 2.5$ns.
4. The outputs are measured one at a time with one transition per measurement.

Switch Positions

Test	Switch
t_{PLZ}, t_{PZL} (output on I-side)	6.0V
t_{PHZ}, t_{PZH} (output on I-side)	GND
Prop Delay	Open

Test Circuit for Dynamic Electrical Characteristics

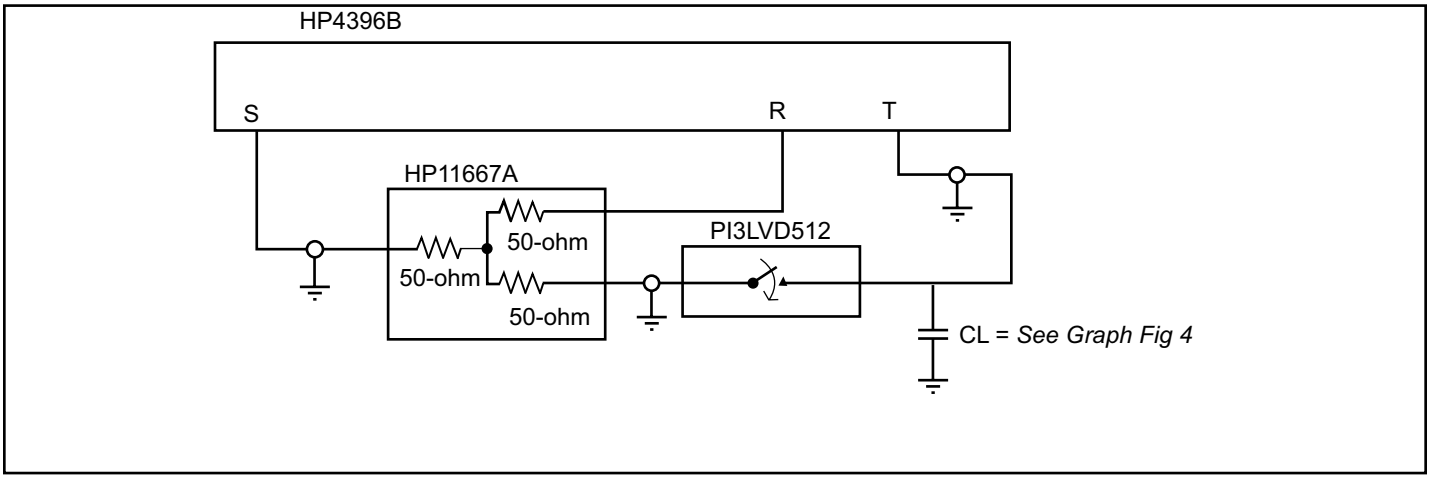


Figure 1. Bandwidth -3dB Testing

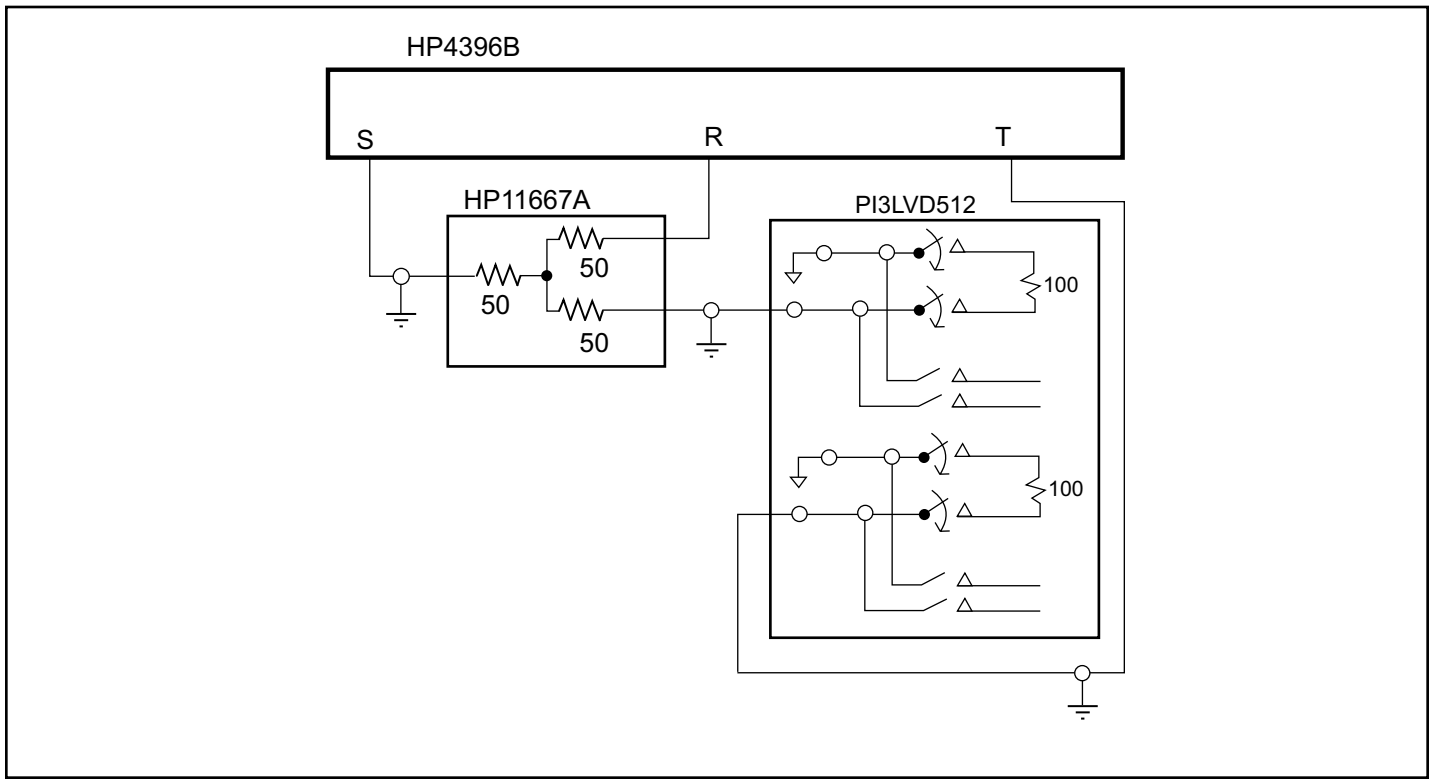


Figure 2. Crosstalk Test Setup

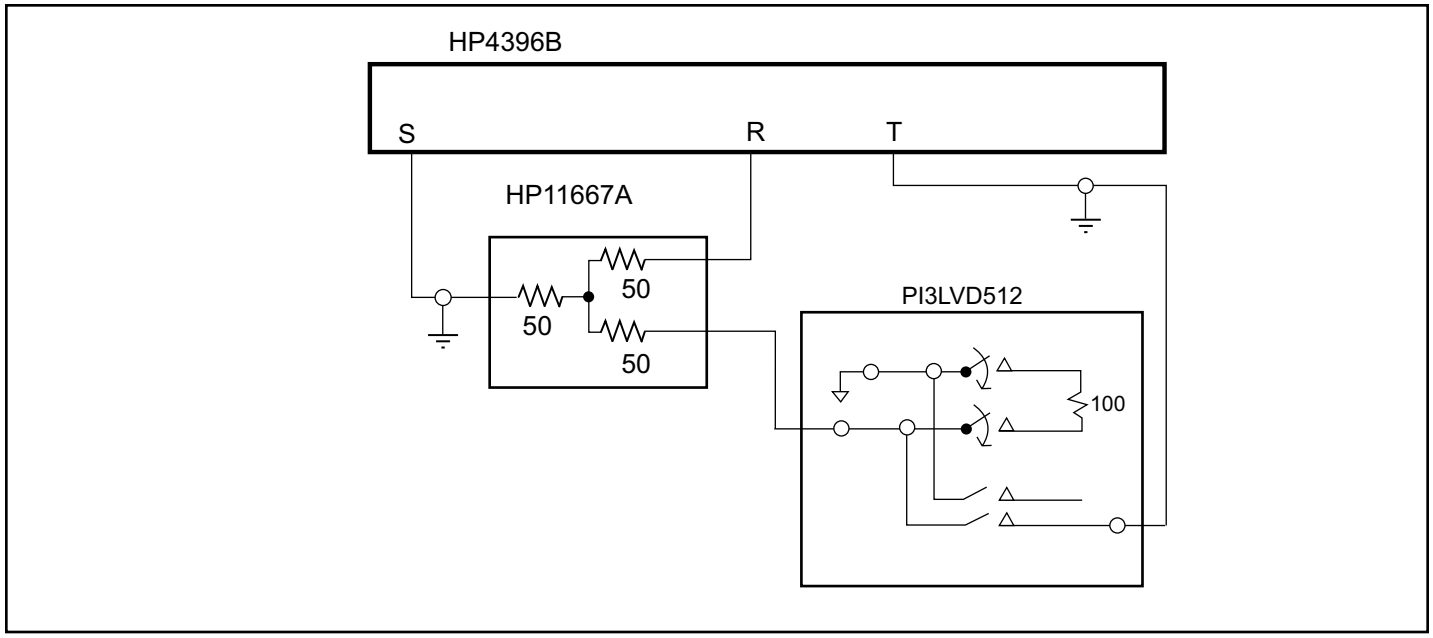
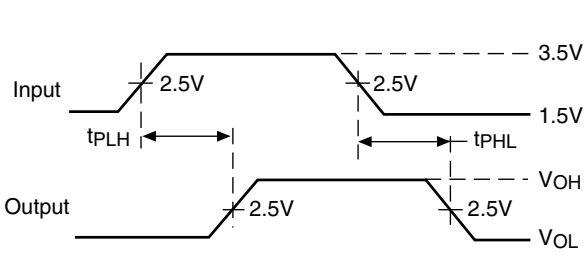
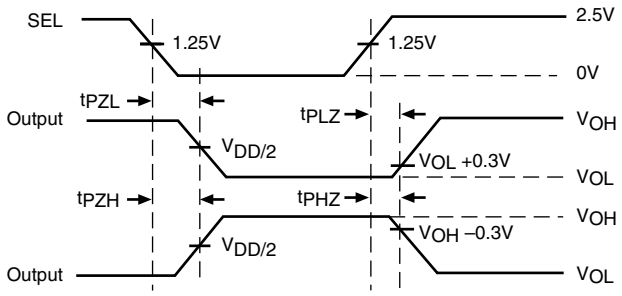


Figure 3. Off Isolation Test Setup

Switching Waveforms



Voltage Waveforms Propagation Delay Times



Voltage Waveforms Enable and Disable Times

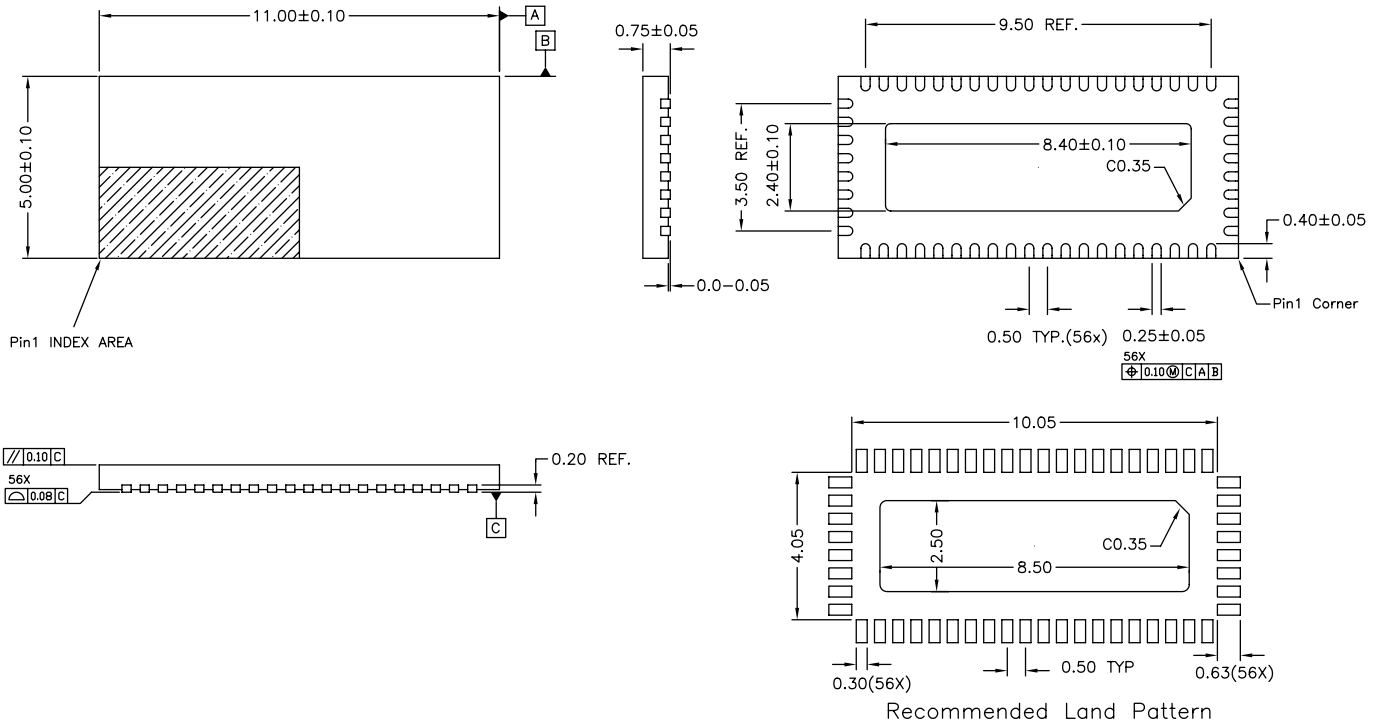
Applications Information

Logic Inputs

The logic control inputs can be driven up to +3.6V regardless of the supply voltage. For example, given a +3.3V supply, the output enables or select pins may be driven low to 0V and high to 3.6V. Driving IN Rail-to-Rail® minimizes power consumption.

Rail-to-Rail is a registered trademark of Nippon Motorola, Ltd

Packaging Mechanical: 56-Pin TQFN (ZF)

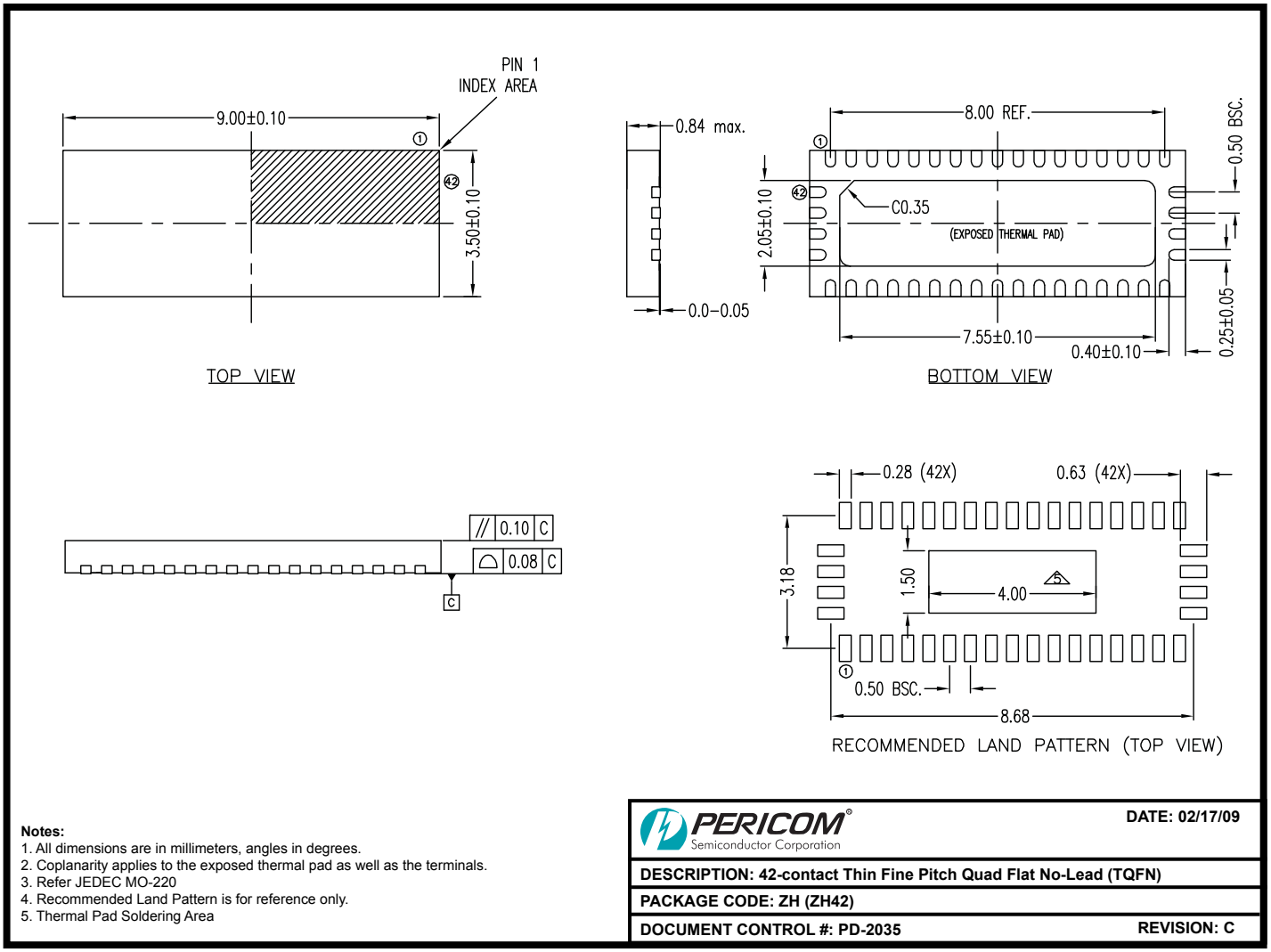


NOTE :
1. ALL DIMENSION ARE IN mm. ANGLES IN DEGREES.
2. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
3. REFER JEDEC MO−220 MODIFIED.
4. Thermal Via Diameter. Recommended 0.2~0.33mm
5. Thermal Via Pitch. Recommended 1.27mm

PERICOM Semiconductor Corporation	DATE: 05/15/08
DESCRIPTION: 56-contact, Thin Fine Pitch Quad Flat No-lead (TQFN)	
PACKAGE CODE: ZF56	
DOCUMENT CONTROL #: PD-2024	REVISION: C

08-0208

Packaging Mechanical: 42 pin TQFN (ZH)



Notes:
1. All dimensions are in millimeters, angles in degrees.
2. Coplanarity applies to the exposed thermal pad as well as the terminals.
3. Refer JEDEC MO-220
4. Recommended Land Pattern is for reference only.
5. Thermal Pad Soldering Area

PERICOM Semiconductor Corporation — DATE: 02/17/09

DESCRIPTION: 42-contact Thin Fine Pitch Quad Flat No-Lead (TQFN)

PACKAGE CODE: ZH (ZH42)

DOCUMENT CONTROL #: PD-2035 — REVISION: C

09-0116

Ordering Information

Ordering Code	Package Code	Package Description
PI3LVD512ZFE	ZFE	Pb-free & Green, 56-pin TQFN
PI3LVD512ZHE	ZHE	Pb-free and Green, 42-pin TQFN

Notes:
- Thermal characteristics can be found on the company web site at www.pericom.com/packaging/
- E = Pb-free and Green
- Adding X suffix = Tape/Reel