# 74ALVCH32973

## 16-bit bus transceiver and transparant D-type latch with 8 independent buffers

Rev. 3 — 17 January 2013 Product data sheet

## 1. General description

The 74ALVCH32973 is a 16-bit bus transceiver and transparent D-type latch with 8 independent buffers with bus hold inputs and 3-state outputs. It features direction (1DIR, 2DIR), latch enable (1$\overline{\text{LOE}}$, 2$\overline{\text{LOE}}$), transceiver output enable (1$\overline{\text{TOE}}$, 2$\overline{\text{TOE}}$) and latch enable (1LE, 2LE) control inputs; four 8-bit transceiver ports (1An, 2An & 1Bn, 2Bn); two 8-bit D-type latch output ports (1Qn, 2Qn) and an 8-bit buffer with data inputs Dn and outputs Yn. The configuration of the control pins allows the device to be used as one 8-bit buffer, two 8-bit transceivers, and two 8-bit latches or one 8-bit buffer, one 16-bit transceiver and one 16-bit latch.

The 8-bit buffer functions independently of the control inputs. The direction of data transmission between A and B is controlled by nDIR and when n$\overline{\text{TOE}}$ is set HIGH the A and B ports will assume a HIGH-impedance OFF-state, they will be effectively isolated. When nLE is HIGH, data at the A inputs enter the latches. In this condition the latches are transparent, a Q output will change each time its corresponding A-input changes. When nLE is LOW the latches store the information that was present at the inputs a set-up time preceding the HIGH-to-LOW transition of nLE. A HIGH on n$\overline{\text{LOE}}$ causes the Q outputs to assume a high-impedance OFF-state. Operation of the n$\overline{\text{LOE}}$ input does not affect the state of the latches.

## 2. Features and benefits

- Wide supply voltage range from 1.2 V to 3.6 V
- Complies with JEDEC standard JESD8-B
- CMOS low power consumption
- Direct interface with TTL levels
- All data inputs have bus hold
- Output drive capability 50 Ω transmission lines at 85 °C
- Current drive ±24 mA at $V_{CC}$ = 3.0 V

## 3. Ordering information

**Table 1. Ordering information**

| Type number | Temperature range | Package | | |
|---|---|---|---|---|
| | | Name | Description | Version |
| 74ALVCH32973EC | −40 °C to +85 °C | LFBGA96 | plastic low profile fine-pitch ball grid array package; 96 balls; body 13.5 × 5.5 × 1.05 mm | SOT536-1 |

## 4. Functional diagram

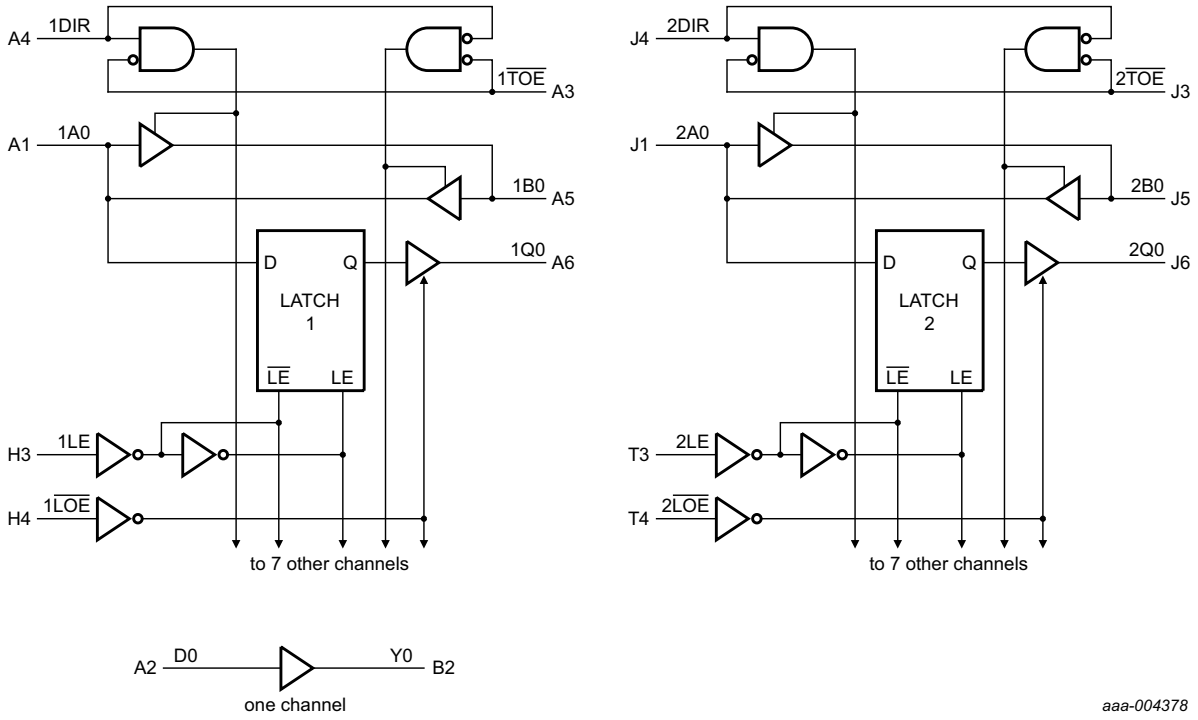



**Fig 1. Logic symbol**

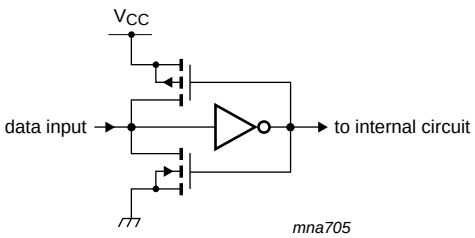



**Fig 2. Bus hold circuit**

# 5. Pinning information

## 5.1 Pinning

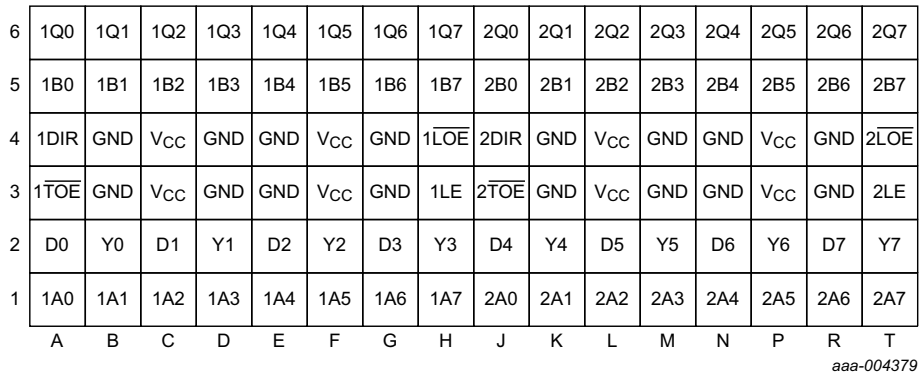



**Fig 3. Pin configuration**

## 5.2 Pin description

**Table 2. Pin description**

| Symbol | Ball | Description |
|---|---|---|
| n$\overline{\text{TOE}}$ (n = 1 to 2) | A3, J3 | transceiver output enable input (active LOW) |
| nDIR (n = 1 to 2) | A4, J4 | direction control input (active HIGH) |
| nLE (n = 1 to 2) | H3, T3 | latch enable input (active HIGH) |
| n$\overline{\text{LOE}}$ (n = 1 to 2) | H4, T4 | latch output enable input (active LOW) |
| 1A[0:7] | A1, B1, C1, D1, E1, F1,G1, H1 | data input/output |
| D[0:7] | A2, C2, E2, G2, J2, L2, N2, R2 | data input |
| 1B[0:7] | A5, B5, C5, D5, E5, F5, G5, H5 | data input/output |
| 2B[0:7] | J5, K5, L5, M5, N5, P5, R5, T5 | data input/output |
| Y[0:7] | B2, D2, F2, H2, K2, M2, P2, T2 | data output |
| 1Q[0:7] | A6, B6, C6, D6, E6, F6, G6, H6 | data output |
| 2A[0:7] | J1, K1, L1, M1, N1, P1, R1, T1 | data input/output |
| 2Q[0:7] | J6, K6, L6, M6, N6, P6, R6, T6 | data output |
| GND | B3, B4, D3, D4, E3, E4, G3, G4, K3, K4, M3, M4, N3, N4, R3, R4 | ground (0 V) |
| $V_{CC}$ | C3, C4, F3, F4, L3, L4, P3, P4 | supply voltage |

# 6. Functional description

## 6.1 Function table

**Table 3. Function table[1]**

| Inputs | | | Internal latches | Outputs nQn | Operating mode |
|---|---|---|---|---|---|
| $\overline{nLOE}$ | nLE | nAn | | | |
| L | H | L | L | L | enable and read register (transparent mode) |
| L | H | H | H | H | |
| L | ↓ | l | L | L | latch and read register |
| L | ↓ | h | H | H | |
| L | L | X | no change | no change | hold mode |
| H | ↓ | l | L | Z | latch register and disable outputs |
| H | ↓ | h | H | Z | |
| H | H | L | L | Z | enable register and disable outputs |
| H | H | H | H | Z | |
| H | L | X | no change | Z | hold mode and disable outputs |

[1] H = HIGH voltage level;
L = LOW voltage level;
h = HIGH voltage level one set-up time prior to the HIGH-to-LOW LE transition;
l = LOW voltage level one set-up time prior to the HIGH-to-LOW LE transition;
↓ = negative-going transition;
Z = high-impedance OFF-state;
X = don't care.

**Table 4. Function table[1]**

| Inputs | | Outputs | |
|---|---|---|---|
| $\overline{nTOE}$ | nDIR | nAn | nBn |
| L | L | nAn = nBn | input |
| L | H | input | nBn = nAn |
| H | X | Z | Z |

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

**Table 5. Function table[1]**

| Input | Output |
|---|---|
| Dn | Yn |
| L | L |
| H | H |

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

# 7. Limiting values

**Table 6. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).*

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{CC}$ | supply voltage | | | –0.5 | +4.6 | V |
| $I_{IK}$ | input clamping current | $V_I < 0$ V | | –50 | - | mA |
| $V_I$ | input voltage | control inputs | [1] | –0.5 | +4.6 | V |
| | | data inputs | [1] | –0.5 | $V_{CC}$ + 0.5 | V |
| $I_{OK}$ | output clamping current | $V_O > V_{CC}$ or $V_O < 0$ V | | - | ±50 | mA |
| $V_O$ | output voltage | | [1] | –0.5 | $V_{CC}$ + 0.5 | V |
| $I_O$ | output current | $V_O$ = 0 V to $V_{CC}$ | | - | ±50 | mA |
| $I_{CC}$ | supply current | | | - | 100 | mA |
| $I_{GND}$ | ground current | | | –100 | - | mA |
| $T_{stg}$ | storage temperature | | | –65 | +150 | °C |
| $P_{tot}$ | total power dissipation | $T_{amb}$ = –40 °C to +85 °C | [2] | - | 1000 | mW |

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] Above 70 °C the value of $P_{tot}$ derates linearly with 1.8 mW/K.

# 8. Recommended operating conditions

**Table 7. Recommended operating conditions**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{CC}$ | supply voltage | maximum speed performance | | | | |
| | | $C_L$ = 30 pF | 2.3 | - | 2.7 | V |
| | | $C_L$ = 50 pF | 3.0 | - | 3.6 | V |
| | | low voltage applications | 1.2 | - | 3.6 | V |
| $V_I$ | input voltage | | 0 | - | $V_{CC}$ | V |
| $V_O$ | output voltage | | 0 | - | $V_{CC}$ | V |
| $T_{amb}$ | ambient temperature | in free air | –40 | - | +85 | °C |
| $\Delta t/\Delta V$ | input transition rise and fall rate | $V_{CC}$ = 2.3 V to 3.0 V | 0 | - | 20 | ns/V |
| | | $V_{CC}$ = 3.0 V to 3.6 V | 0 | - | 10 | ns/V |

# 9. Static characteristics

**Table 8. Static characteristics**

*At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).*

| Symbol | Parameter | Conditions | Min | Typ[1] | Max | Unit |
|---|---|---|---|---|---|---|
| **$T_{amb}$ = –40 °C to +85 °C** | | | | | | |
| $V_{IH}$ | HIGH-level input voltage | $V_{CC}$ = 1.2 V | $V_{CC}$ | - | - | V |
| | | $V_{CC}$ = 1.8 V | 0.7$V_{CC}$ | 0.9 | - | V |
| | | $V_{CC}$ = 2.3 V to 2.7 V | 1.7 | 1.2 | - | V |
| | | $V_{CC}$ = 2.7 V to 3.6 V | 2.0 | 1.5 | - | V |
| $V_{IL}$ | LOW-level input voltage | $V_{CC}$ = 1.2 V | - | - | 0 | V |
| | | $V_{CC}$ = 1.8 V | - | 0.9 | 0.2$V_{CC}$ | V |
| | | $V_{CC}$ = 2.3 V to 2.7 V | - | 1.2 | 0.7 | V |
| | | $V_{CC}$ = 2.7 V to 3.6 V | - | 1.5 | 0.8 | V |
| $V_{OH}$ | HIGH-level output voltage | $V_I$ = $V_{IH}$ or $V_{IL}$ | | | | |
| | | $I_O$ = –100 μA; $V_{CC}$ = 1.8 V to 3.6 V | $V_{CC}$ – 0.2 | $V_{CC}$ | - | V |
| | | $I_O$ = –6 mA; $V_{CC}$ = 1.8 V | $V_{CC}$ – 0.4 | $V_{CC}$ – 0.1 | - | V |
| | | $I_O$ = –6 mA; $V_{CC}$ = 2.3 V | $V_{CC}$ – 0.3 | $V_{CC}$ – 0.08 | - | V |
| | | $I_O$ = –12 mA; $V_{CC}$ = 2.3 V | $V_{CC}$ – 0.5 | $V_{CC}$ – 0.17 | - | V |
| | | $I_O$ = –12 mA; $V_{CC}$ = 2.7 V | $V_{CC}$ – 0.5 | $V_{CC}$ – 0.14 | - | V |
| | | $I_O$ = –18 mA; $V_{CC}$ = 2.3 V | $V_{CC}$ – 0.6 | $V_{CC}$ – 0.26 | - | V |
| | | $I_O$ = –24 mA; $V_{CC}$ = 3.0 V | $V_{CC}$ – 1.0 | $V_{CC}$ – 0.28 | - | V |
| $V_{OL}$ | LOW-level output voltage | $V_I$ = $V_{IH}$ or $V_{IL}$ | | | | |
| | | $I_O$ = 100 μA; $V_{CC}$ = 1.8 V to 3.6 V | - | 0 | 0.20 | V |
| | | $I_O$ = 6 mA; $V_{CC}$ = 1.8 V | - | 0.09 | 0.30 | V |
| | | $I_O$ = 6 mA; $V_{CC}$ = 2.3 V | - | 0.07 | 0.20 | V |
| | | $I_O$ = 12 mA; $V_{CC}$ = 2.3 V | - | 0.15 | 0.40 | V |
| | | $I_O$ = 12 mA; $V_{CC}$ = 2.7 V | - | 0.14 | 0.40 | V |
| | | $I_O$ = 18 mA; $V_{CC}$ = 2.3 V | - | 0.23 | 0.60 | V |
| | | $I_O$ = 24 mA; $V_{CC}$ = 3.0 V | - | 0.27 | 0.55 | V |
| $I_I$ | input leakage current | $V_{CC}$ = 1.8 V to 3.6 V; $V_I$ = $V_{CC}$ or GND | - | 0.1 | 5 | μA |
| $I_{OZ}$ | OFF-state output current | $V_I$ = $V_{IH}$ or $V_{IL}$; $V_O$ = $V_{CC}$ or GND | | | | |
| | | $V_{CC}$ = 1.8 V to 2.7 V | - | 0.1 | 5 | μA |
| | | $V_{CC}$ = 2.7 V to 3.6 V | - | 0.1 | 10 | μA |
| $I_{CC}$ | supply current | $V_I$ = $V_{CC}$ or GND; $I_O$ = 0 A; | | | | |
| | | $V_{CC}$ = 1.8 V to 2.7 V | - | 0.4 | 80 | μA |
| | | $V_{CC}$ = 2.7 V to 3.6 V | - | 0.4 | 80 | μA |
| $\Delta I_{CC}$ | additional supply current | $V_I$ = $V_{CC}$ – 0.6 V; $I_O$ = 0 A; $V_{CC}$ = 2.7 V to 3.6 V | | | | |
| | | per control input | - | 5 | 500 | μA |
| | | per data I/O input | - | 150 | 750 | μA |
| $I_{BHL}$ | bus hold LOW current | $V_{CC}$ = 2.3 V; $V_I$ = 0.7 V | 45 | - | - | μA |
| | | $V_{CC}$ = 3.0 V; $V_I$ = 0.8 V | 75 | 150 | - | μA |

**Table 8. Static characteristics** *...continued*

*At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).*

| Symbol | Parameter | Conditions | Min | Typ[1] | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{BHH}$ | bus hold HIGH current | $V_{CC}$ = 2.3 V; $V_I$ = 1.7 V | –45 | - | - | μA |
| | | $V_{CC}$ = 3.0 V; $V_I$ = 2.0 V | –75 | –175 | - | μA |
| $I_{BHLO}$ | bus hold LOW overdrive current | $V_{CC}$ = 3.6 V | 500 | - | - | μA |
| $I_{BHHO}$ | bus hold HIGH overdrive current | $V_{CC}$ = 3.6 V | –500 | - | - | μA |
| $C_I$ | input capacitance | | - | 5.0 | - | pF |
| $C_{I/O}$ | input/output capacitance | | - | 8.0 | - | pF |

[1] All typical values are measured at $T_{amb}$ = 25 °C.

# 10. Dynamic characteristics

**Table 9. Dynamic characteristics**

*At recommended operating conditions. Voltages are referenced to GND (ground = 0 V); test circuit Figure 10.*

| Symbol | Parameter | Conditions | | Min | Typ[1] | Max | Unit |
|---|---|---|---|---|---|---|---|
| **$T_{amb}$ = –40 °C to +85 °C** | | | | | | | |
| $t_{pd}$ | propagation delay | nAn to nQn; see Figure 4 | [2] | | | | |
| | | $V_{CC}$ = 1.2 V | | - | 7.0 | - | ns |
| | | $V_{CC}$ = 1.8 V | | 1.1 | 3.4 | 5.7 | ns |
| | | $V_{CC}$ = 2.3 V to 2.7 V | [3] | 1.0 | 2.2 | 3.9 | ns |
| | | $V_{CC}$ = 2.7 V | | 1.0 | 2.7 | 3.8 | ns |
| | | $V_{CC}$ = 3.0 V to 3.6 V | [4] | 1.0 | 2.5 | 3.6 | ns |
| | | nLE to nQn; see Figure 5 | [2] | | | | |
| | | $V_{CC}$ = 1.2 V | | - | 8.2 | - | ns |
| | | $V_{CC}$ = 1.8 V | | 1.5 | 3.7 | 5.9 | ns |
| | | $V_{CC}$ = 2.3 V to 2.7 V | [3] | 1.0 | 2.4 | 3.8 | ns |
| | | $V_{CC}$ = 2.7 V | | 1.0 | 2.7 | 4.3 | ns |
| | | $V_{CC}$ = 3.0 V to 3.6 V | [4] | 0.8 | 2.6 | 4.1 | ns |
| | | nAn to nBn or nBn to nAn; see Figure 6 | [2] | | | | |
| | | $V_{CC}$ = 1.2 V | | - | 5.9 | - | ns |
| | | $V_{CC}$ = 1.8 V | | 1.4 | 3.0 | 4.3 | ns |
| | | $V_{CC}$ = 2.3 V to 2.7 V | [3] | 1.0 | 2.0 | 3.8 | ns |
| | | $V_{CC}$ = 2.7 V | | 1.0 | 2.3 | 3.7 | ns |
| | | $V_{CC}$ = 3.0 V to 3.6 V | [4] | 1.0 | 2.2 | 3.4 | ns |
| | | Dn to Yn; see Figure 7 | [2] | | | | |
| | | $V_{CC}$ = 1.2 V | | - | 4.6 | - | ns |
| | | $V_{CC}$ = 1.8 V | | 1.1 | 2.4 | 5.1 | ns |
| | | $V_{CC}$ = 2.3 V to 2.7 V | [3] | 0.7 | 1.7 | 3.7 | ns |
| | | $V_{CC}$ = 2.7 V | | 1.0 | 2.1 | 3.6 | ns |
| | | $V_{CC}$ = 3.0 V to 3.6 V | [4] | 0.9 | 1.8 | 3.1 | ns |

**Table 9. Dynamic characteristics** *...continued*

*At recommended operating conditions. Voltages are referenced to GND (ground = 0 V); test circuit Figure 10.*

| Symbol | Parameter | Conditions | | Min | Typ[1] | Max | Unit |
|---|---|---|---|---|---|---|---|
| $t_{en}$ | enable time | $n\overline{LOE}$ to nQn; see Figure 8 | [2] | | | | |
| | | $V_{CC}$ = 1.2 V | | - | 9.5 | - | ns |
| | | $V_{CC}$ = 1.8 V | | 1.5 | 4.6 | 7.3 | ns |
| | | $V_{CC}$ = 2.3 V to 2.7 V | [3] | 1.0 | 3.0 | 5.2 | ns |
| | | $V_{CC}$ = 2.7 V | | 1.0 | 3.3 | 4.9 | ns |
| | | $V_{CC}$ = 3.0 V to 3.6 V | [4] | 1.0 | 2.7 | 4.3 | ns |
| | | $n\overline{TOE}$ to nAn or nBn; see Figure 8 | [2] | | | | |
| | | $V_{CC}$ = 1.2 V | | - | 10.0 | - | ns |
| | | $V_{CC}$ = 1.8 V | | 1.5 | 4.7 | 7.6 | ns |
| | | $V_{CC}$ = 2.3 V to 2.7 V | [3] | 1.0 | 3.2 | 5.7 | ns |
| | | $V_{CC}$ = 2.7 V | | 1.0 | 3.3 | 5.4 | ns |
| | | $V_{CC}$ = 3.0 V to 3.6 V | [4] | 1.0 | 2.7 | 4.4 | ns |
| | | nDIR to nAn or nBn; see Figure 8 | [2] | | | | |
| | | $V_{CC}$ = 1.2 V | | - | 7.0 | - | ns |
| | | $V_{CC}$ = 1.8 V | | 1.5 | 3.5 | 7.6 | ns |
| | | $V_{CC}$ = 2.3 V to 2.7 V | [3] | 1.0 | 2.7 | 5.2 | ns |
| | | $V_{CC}$ = 2.7 V | | 1.0 | 4.2 | 6.0 | ns |
| | | $V_{CC}$ = 3.0 V to 3.6 V | [4] | 1.0 | 3.4 | 5.0 | ns |
| $t_{dis}$ | disable time | $n\overline{LOE}$ to nQn; see Figure 8 | [2] | | | | |
| | | $V_{CC}$ = 1.2 V | | - | 6.7 | - | ns |
| | | $V_{CC}$ = 1.8 V | | 1.5 | 3.5 | 5.6 | ns |
| | | $V_{CC}$ = 2.3 V to 2.7 V | [3] | 1.0 | 2.2 | 4.1 | ns |
| | | $V_{CC}$ = 2.7 V | | 1.0 | 3.4 | 4.7 | ns |
| | | $V_{CC}$ = 3.0 V to 3.6 V | [4] | 1.0 | 3.1 | 4.2 | ns |
| | | $n\overline{TOE}$ to nAn or nBn; see Figure 8 | [2] | | | | |
| | | $V_{CC}$ = 1.2 V | | - | 7.0 | - | ns |
| | | $V_{CC}$ = 1.8 V | | 1.5 | 3.6 | 7.6 | ns |
| | | $V_{CC}$ = 2.3 V to 2.7 V | [3] | 1.0 | 2.6 | 5.2 | ns |
| | | $V_{CC}$ = 2.7 V | | 1.0 | 3.5 | 4.6 | ns |
| | | $V_{CC}$ = 3.0 V to 3.6 V | [4] | 1.0 | 3.2 | 4.3 | ns |
| | | nDIR to nAn or nBn; see Figure 8 | [2] | | | | |
| | | $V_{CC}$ = 1.2 V | | - | 7.2 | - | ns |
| | | $V_{CC}$ = 1.8 V | | 1.5 | 3.7 | 7.6 | ns |
| | | $V_{CC}$ = 2.3 V to 2.7 V | [3] | 1.0 | 2.7 | 5.2 | ns |
| | | $V_{CC}$ = 2.7 V | | 1.0 | 4.0 | 6.0 | ns |
| | | $V_{CC}$ = 3.0 V to 3.6 V | [4] | 1.0 | 3.2 | 5.0 | ns |

**Table 9. Dynamic characteristics** *...continued*

*At recommended operating conditions. Voltages are referenced to GND (ground = 0 V); test circuit Figure 10.*

| Symbol | Parameter | Conditions | | Min | Typ[1] | Max | Unit |
|---|---|---|---|---|---|---|---|
| $t_W$ | pulse width | nLE HIGH; see Figure 5 | | | | | |
| | | $V_{CC}$ = 1.8 V | | 3.5 | 1.0 | - | ns |
| | | $V_{CC}$ = 2.3 V to 2.7 V | [3] | 3.0 | 1.0 | - | ns |
| | | $V_{CC}$ = 2.7 V | | 3.0 | 1.0 | - | ns |
| | | $V_{CC}$ = 3.0 V to 3.6 V | [4] | 2.5 | 1.0 | - | ns |
| $t_{su}$ | set-up time | nAn to nLE; see Figure 9 | | | | | |
| | | $V_{CC}$ = 1.8 V | | 1.1 | –0.1 | - | ns |
| | | $V_{CC}$ = 2.3 V to 2.7 V | [3] | 1.1 | –0.1 | - | ns |
| | | $V_{CC}$ = 2.7 V | | 1.1 | –0.1 | - | ns |
| | | $V_{CC}$ = 3.0 V to 3.6 V | [4] | 1.1 | –0.1 | - | ns |
| $t_h$ | hold time | nAn to nLE; see Figure 9 | | | | | |
| | | $V_{CC}$ = 1.8 V | | 1.3 | 0.1 | - | ns |
| | | $V_{CC}$ = 2.3 V to 2.7 V | [3] | 1.6 | 0.2 | - | ns |
| | | $V_{CC}$ = 2.7 V | | 1.6 | 0.4 | - | ns |
| | | $V_{CC}$ = 3.0 V to 3.6 V | [4] | 1.3 | 0.2 | - | ns |
| $C_{PD}$ | power dissipation capacitance | per latch or buffer; $V_I$ = GND to $V_{CC}$; $V_{CC}$ = 1.2 V to 3.6 V | [5] | | | | |
| | | Q outputs enabled; A and B ports isolated; $f_{i(nAn)}$ = 10 MHz; $f_{i(nLE)}$ = 20 MHz; $f_{i(nQn)}$ = 10 MHz | | - | 26 | - | pF |
| | | A outputs enabled; Q output disabled; $f_{i(nAn)}$ = 10 MHz; $f_{i(nBn)}$ = 10 MHz | | - | 16 | - | pF |
| | | B outputs enabled; Q output disabled; $f_{i(nAn)}$ = 10 MHz; $f_{i(nBn)}$ = 10 MHz | | - | 16 | - | pF |
| | | Y outputs enabled; A and B parts isolated; Q output disabled; $f_{i(Dn)}$ = 10 MHz; $f_{i(Yn)}$ = 10 MHz | | - | 12 | - | pF |
| | | all outputs disabled; one nLE input and one nAn input switching; $f_{i(nAn)}$ = 10 MHz; $f_{i(nLE)}$ = 20 MHz; $f_{i(nQn)}$ = 0 MHz | | - | 18 | - | pF |
| | | Q outputs disabled; A and B ports isolated; one nLE input switching; $f_{i(nAn)}$ = 0 MHz; $f_{i(nLE)}$ = 20 MHz; $f_{i(nQn)}$ = 0 MHz | | - | 6 | - | pF |

[1] All typical values are measured at $T_{amb}$ = 25 °C.

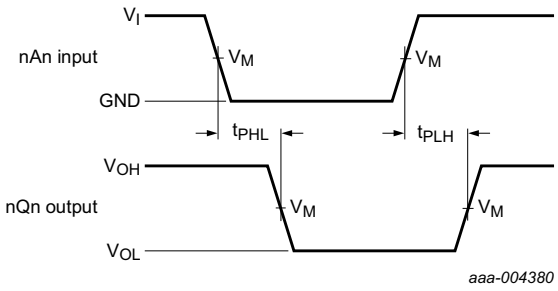
[2] $t_{pd}$ is the same as $t_{PLH}$ and $t_{PHL}$.
$t_{en}$ is the same as $t_{PZL}$ and $t_{PZH}$.
$t_{dis}$ is the same as $t_{PLZ}$ and $t_{PHZ}$.

[3] Typical values are measured at $V_{CC}$ = 2.5 V.

[4] Typical values are measured at $V_{CC}$ = 3.3 V.

[5] $C_{PD}$ is used to determine the dynamic power dissipation ($P_D$ in μW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
$f_i$ = input frequency in MHz; $f_o$ = output frequency in MHz;
$C_L$ = output load capacitance in pF;
$V_{CC}$ = supply voltage in Volts;
N = number of inputs switching;
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

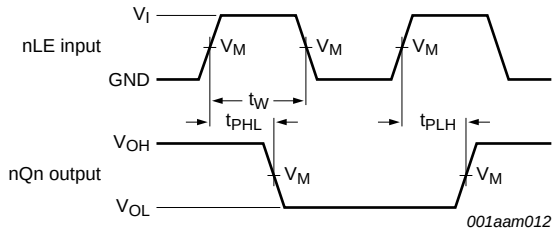
## 11. Waveforms




Measurement points are given in Table 10.

$V_{OL}$ and $V_{OH}$ are typical output levels that occur with the output load.

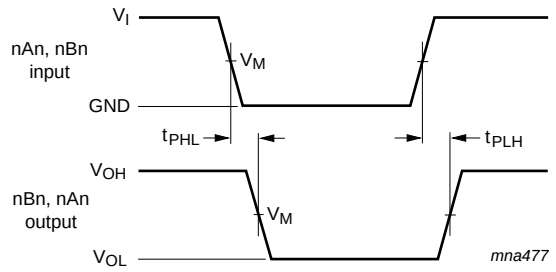
**Fig 4. Propagation delay, input (nAn) to data output (nQn)**




Measurement points are given in Table 10.

$V_{OL}$ and $V_{OH}$ are typical output levels that occur with the output load.

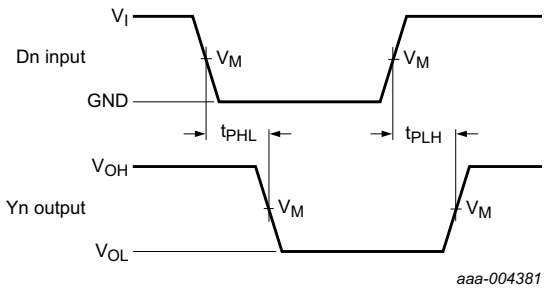
**Fig 5. Propagation delay, latch enable input (nLE) to data output (nQn), and pulse width**




Measurement points are given in Table 10.

$V_{OL}$ and $V_{OH}$ are typical output levels that occur with the output load.

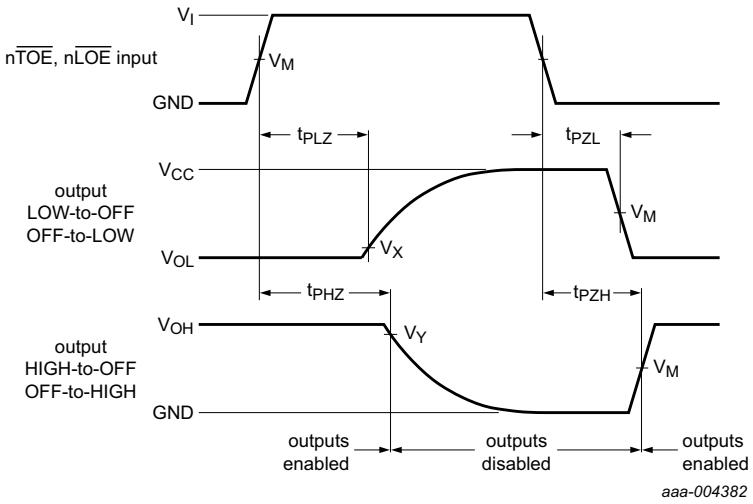
**Fig 6. Propagation delay, input (nAn, nBn) to data output (nBn,nAn)**




Measurement points are given in Table 10.

$V_{OL}$ and $V_{OH}$ are typical output levels that occur with the output load.

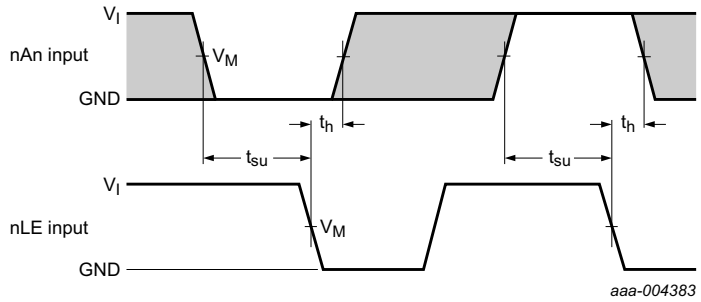
**Fig 7. Propagation delay, input (Dn) to data output (Yn)**




Measurement points are given in Table 10.

$V_{OL}$ and $V_{OH}$ are typical output levels that occur with the output load.

**Fig 8. 3-state enable and disable times**




Measurement points are given in Table 10.

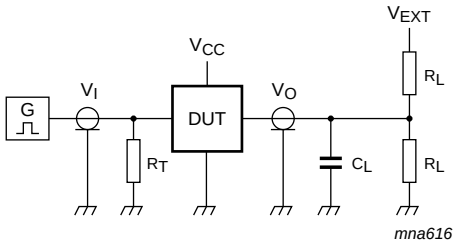
The shaded areas indicate when the input is permitted to change for predictable output performance.

**Fig 9. Data setup and hold times for input (nAn) to input (nLE)**

**Table 10. Measurement points**

| Supply voltage | Input | | Output | | |
|---|---|---|---|---|---|
| $V_{CC}$ | $V_I$ | $V_M$ | $V_M$ | $V_X$ | $V_Y$ |
| 2.3 V to 2.7 V and < 2.3 V | $V_{CC}$ | $0.5 \times V_{CC}$ | $0.5 \times V_{CC}$ | $V_{OL}$ + 0.15 V | $V_{OH}$ − 0.15 V |
| 2.7 V | 2.7 V | 1.5 V | 1.5 V | $V_{OL}$ + 0.3 V | $V_{OH}$ − 0.3 V |
| 3.0 V to 3.6 V | 2.7 V | 1.5 V | 1.5 V | $V_{OL}$ + 0.3 V | $V_{OH}$ − 0.3 V |

## 12. Test information




Test data is given in Table 11.

Definitions for test circuit:

$R_L$ = Load resistance.

$C_L$ = Load capacitance including jig and probe capacitance.

$R_T$ = Termination resistance should be equal to output impedance $Z_o$ of the pulse generator.

$V_{EXT}$ = External voltage for measuring switching times.

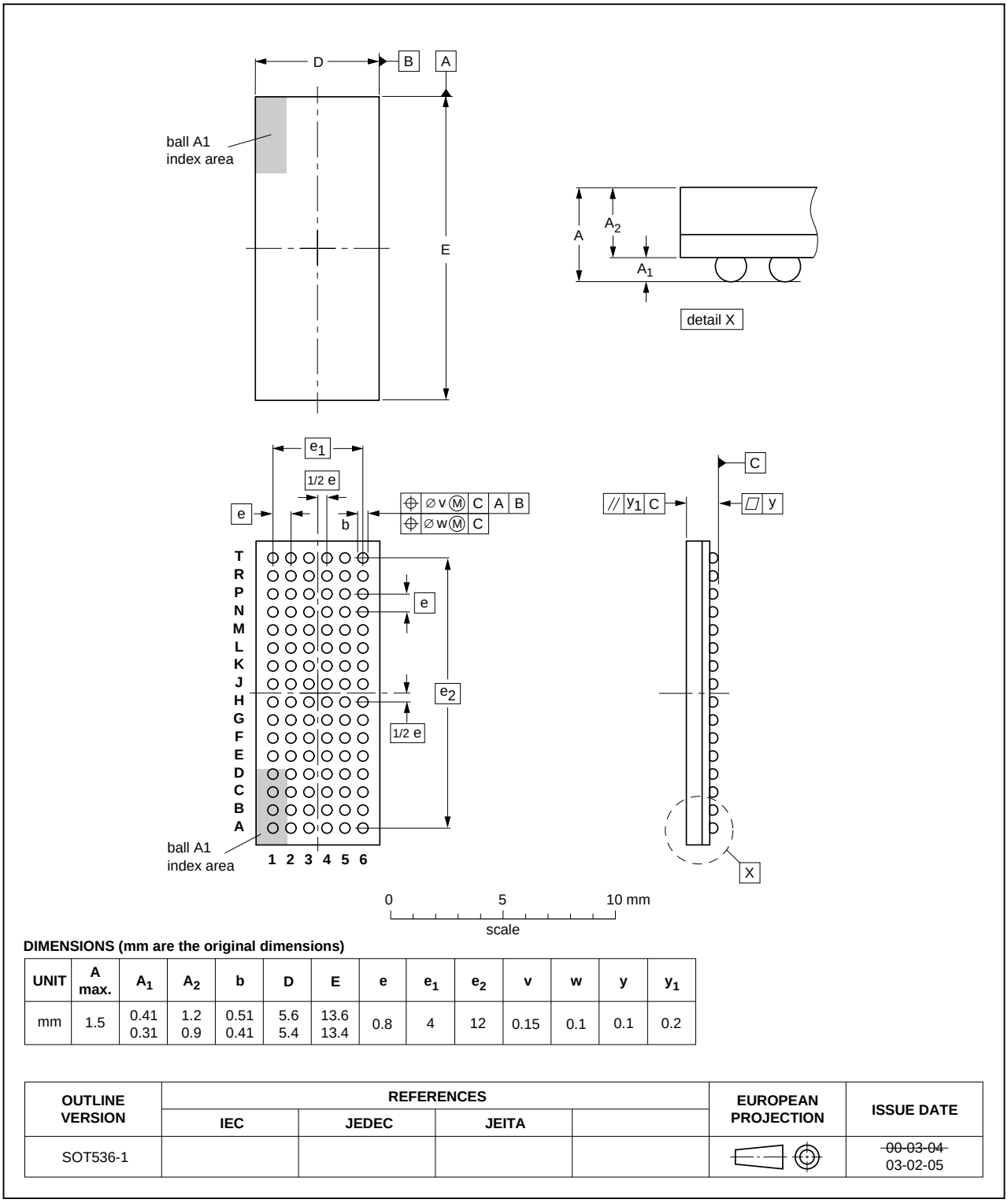
**Fig 10. Test circuit for measuring switching times**

**Table 11. Test data**

| Supply voltage | Input | | Load | | $V_{EXT}$ | | |
|---|---|---|---|---|---|---|---|
| $V_{CC}$ | $V_I$ | $t_r$, $t_f$ | $C_L$ | $R_L$ | $t_{PLH}$, $t_{PHL}$ | $t_{PLZ}$, $t_{PZL}$ | $t_{PHZ}$, $t_{PZH}$ |
| 2.3 V to 2.7 V and < 2.3 V | $V_{CC}$ | ≤ 2.0 ns | 30 pF | 500 Ω | open | $2 \times V_{CC}$ | GND |
| 2.7 V | 2.7 V | 2.5 ns | 50 pF | 500 Ω | open | $2 \times V_{CC}$ | GND |
| 3.0 V to 3.6 V | 2.7 V | 2.5 ns | 50 pF | 500 Ω | open | $2 \times V_{CC}$ | GND |

## 13. Package outline

**LFBGA96: plastic low profile fine-pitch ball grid array package; 96 balls; body 13.5 x 5.5 x 1.05 mm SOT536-1**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A max. | $A_1$ | $A_2$ | b | D | E | e | $e_1$ | $e_2$ | v | w | y | $y_1$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.5 | 0.41<br>0.31 | 1.2<br>0.9 | 0.51<br>0.41 | 5.6<br>5.4 | 13.6<br>13.4 | 0.8 | 4 | 12 | 0.15 | 0.1 | 0.1 | 0.2 |

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT536-1 | | | | | | ~~00-03-04~~<br>03-02-05 |

**Fig 11. Package outline SOT536-1 (LFBGA96)**

## 14. Abbreviations

**Table 12. Abbreviations**

| Acronym | Description |
|---|---|
| CMOS | Complementary Metal-Oxide Semiconductor |
| DUT | Device Under Test |
| TTL | Transistor-Transistor Logic |

## 15. Revision history

**Table 13. Revision history**

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| 74ALVCH32973 v.3 | 20130117 | Product data sheet | - | 74ALVCH32973 v.2 |
| Modifications: | • Table note of function table updated (LOW-to-HIGH changed into HIGH-to-LOW). | | | |
| 74ALVCH32973 v.2 | 20121108 | Product data sheet | - | 74ALVCH32973 v.1 |
| Modifications: | • Function table updated. | | | |
| 74ALVCH32973 v.1 | 20120822 | Product data sheet | - | - |

# 16. Legal information

## 16.1 Data sheet status

| Document status[1][2] | Product status[3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nexperia.com.

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## 18. Contents





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**Date of release: 17 January 2013**