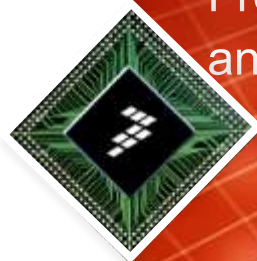




MMPF0100/200 Power Management Integrated Circuit (PMIC) and Other Consumer Analog Product Introduction and Roadmap

AMF-CON-T0605

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September 2013

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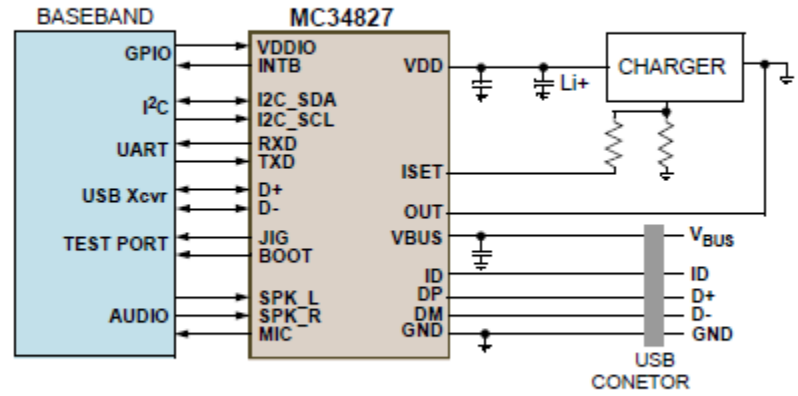
Mini or Micro-USB Interface IC

• FEATURES

- Internal Power Switch Protects the Phone System against 28V Power Supply Input
- Supports USB or UART Test and R/D cables
- High-Speed USB 2.0 Compliant
- Supports 32 ID resistance values with a High-Accuracy 5-bit ADC
- I2C Interface with Interrupt to the Host
- 10µA Quiescent Current in Standby Mode
- 4mm X 3mm 20 Ld. UTQFN and 3mm X 3mm 20 Lead UTQFN Packaging

• BENEFITS

- Flexible input such as ac/dc adapter or USB port
- Sets high or low charging current based on power supply capability
- Supports stereo/mono headsets with or without microphone and remote control



• Applications

- Cell Phones
- MP3/MP4 Players
- Portable Voice Recorders
- USB Universal Charging Solution (UCS-OMTP)
- Supports Mini/Micro - USB Connector
- UART and USB High Speed Communication
- Remote Control/Accessories IDs

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Monolithic Dual H-Bridge for Portable Applications

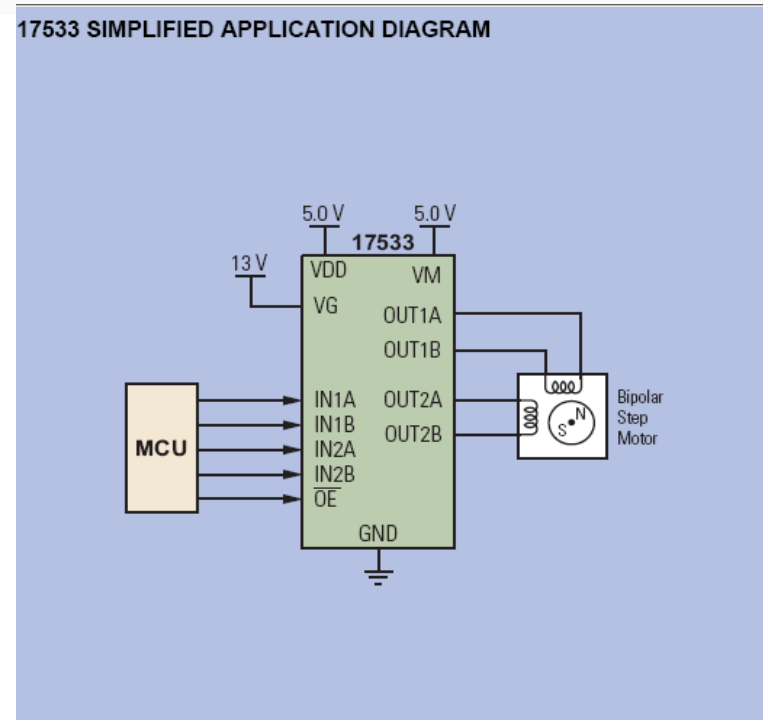
FEATURES

- Motor power supply - 2 to 6.8 V
- Low RDS(ON) 0.8 Ω (typ), 1.4 Ω (Peak)
- Output current 700 mA (DC), 1.4 A (peak)
- 3.0V/5.0V CMOS-Compatible Inputs
- Shoot through current protection circuit
- PWM control input frequency 200 kHz
- Charge pump circuit

BENEFITS

- Simple MCU Interface
- Single or parallel H-Bridge outputs
- Under voltage detection to prevent erratic operation
- Low quiescent current
- Low profile package for portable designs
- Reduces design time

17533 SIMPLIFIED APPLICATION DIAGRAM



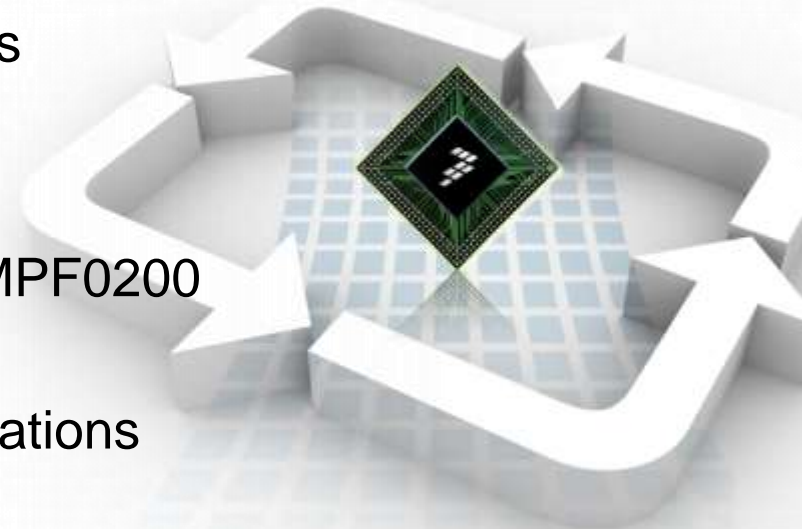
APPLICATIONS

- Portable Electronics
- Lens Shutter Camera
- Optical Disc Drive



Agenda

- *The Warm-up*
 - Role of a PMIC
 - Switching and Linear Regulators
 - Freescale PMIC History
- *The Race*
 - Introducing MMPF0100 and MMPF0200
 - Features
 - Evaluation Tools and Demonstrations
 - Schedule
 - Other Freescale analog power management products
- *The Finish*
 - **Q & A**





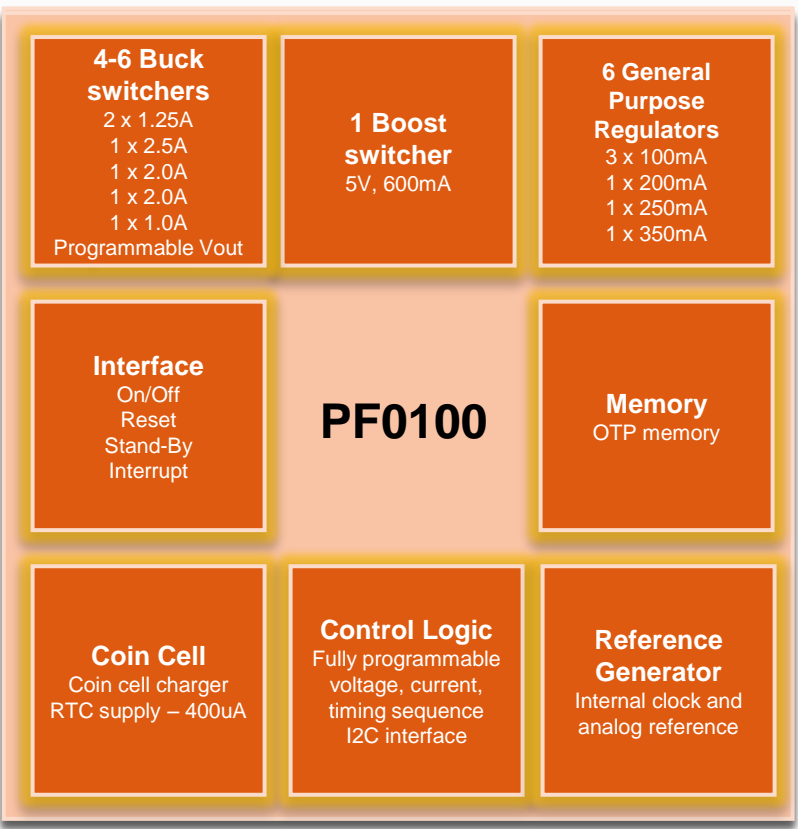


BACKUP



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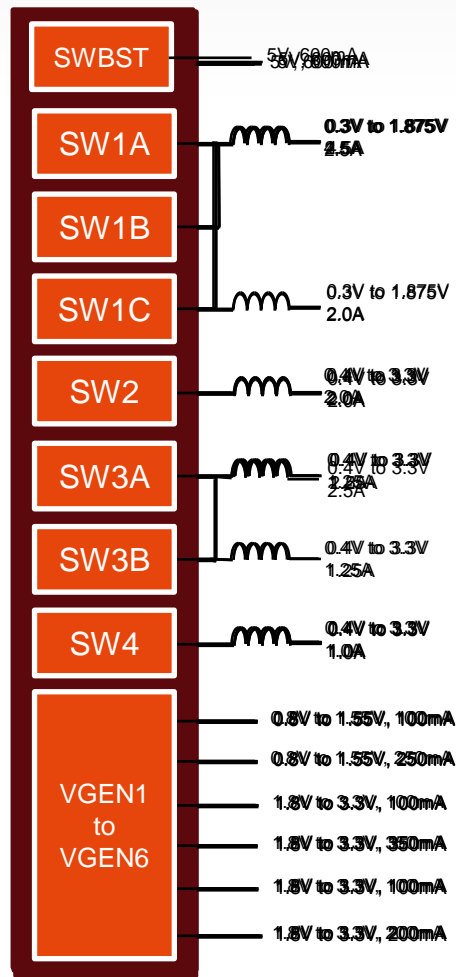
MMPF0100 Buck Regulators



- Input voltage range: 2.8V to 4.5V
- 4 to 6 buck converters
 - (2 x 1.25A, 1 x 2.5A, 1 x 2.0A, 1 x 2.0A, 1 x 1.0A)
 - Single/Multi-phase configurable
- Programmable MOSFET stages to facilitate using smaller inductor
- Programmable current limit (1.5x or 2x rated)
- High light-load efficiency modes (APS/PFM)
- Adjustable switching frequency (1/2/4 MHz options as well as finer frequency margining for EMC)
- High efficiency across entire load range
- Internally compensated thus requiring minimum external components



MPF0100 Buck Regulators – Maximum Configurability



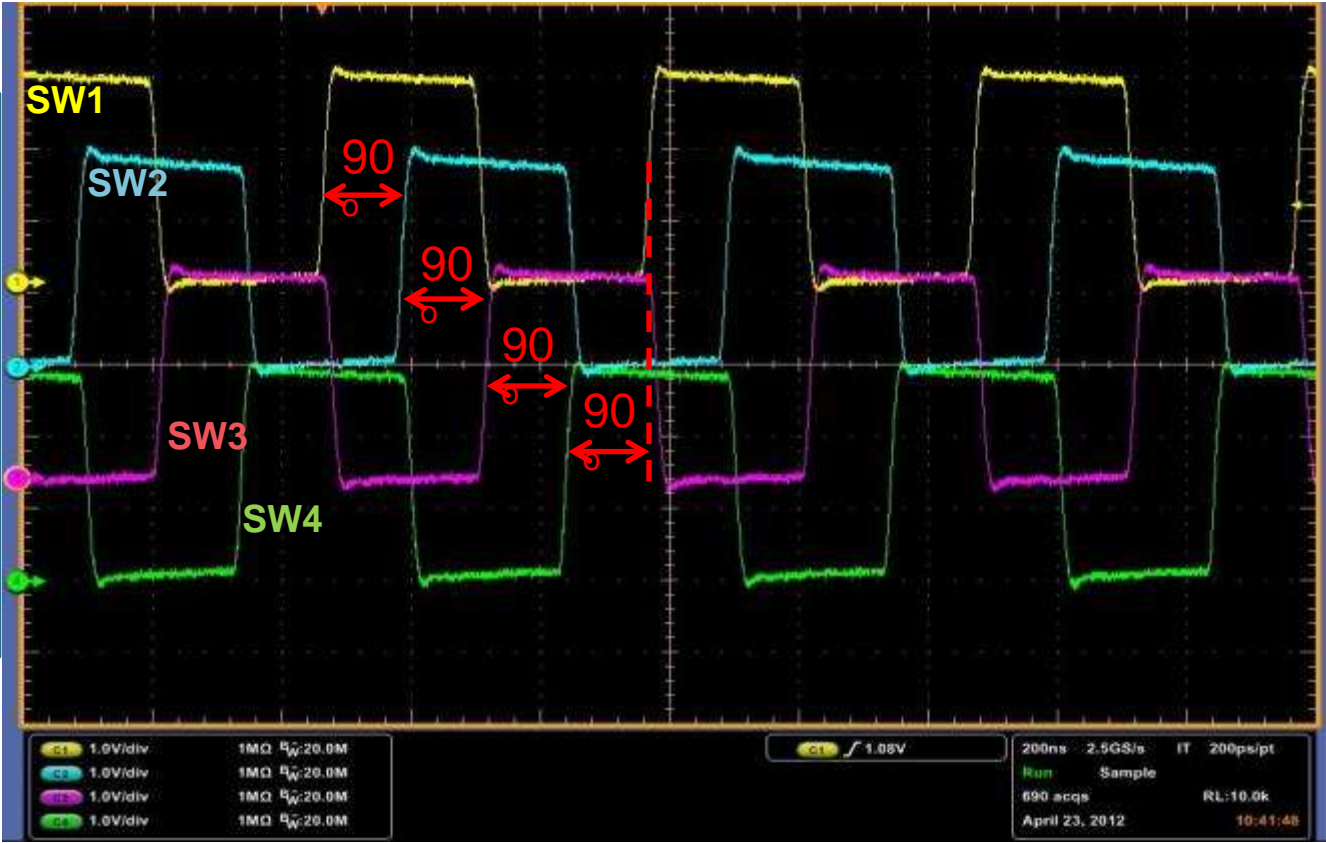
4 Buck, 6 LDO, 1 Boost

Switching Modes and Phase Clock

Operation Modes	Description	Efficiency @ light load	Efficiency @ heavy load
PFM	The regulator is always in PFM mode	high	mid
PWM	The regulator is always in PWM mode	low	high
APS	The regulator moves automatically between Pulse Skip and PWM modes depending on load conditions	high	high

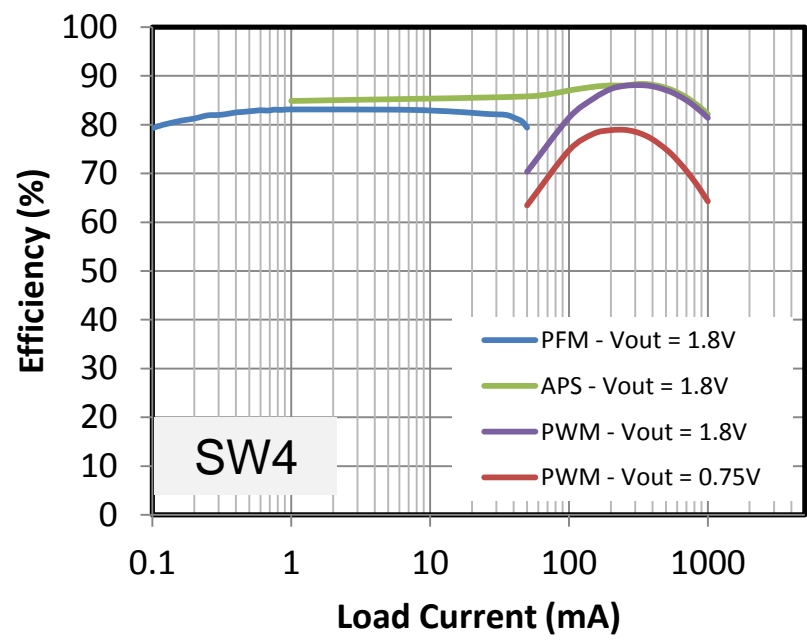
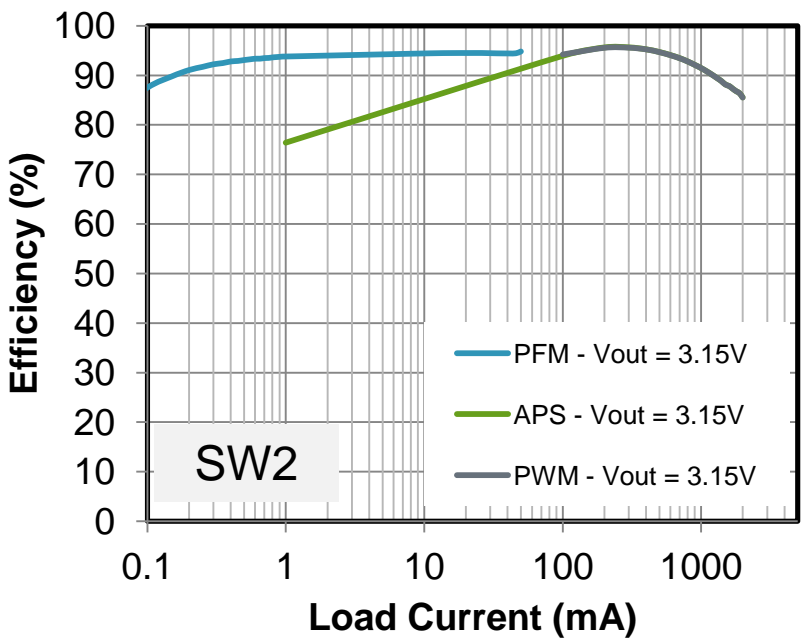
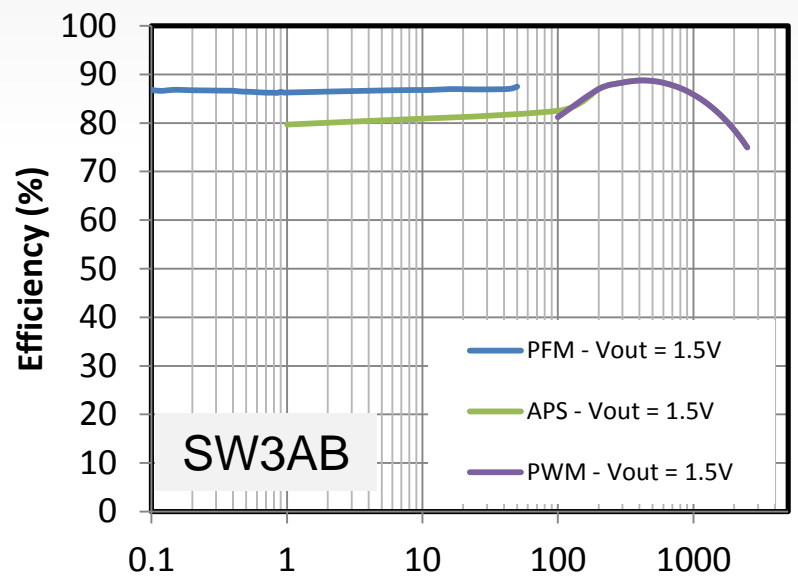
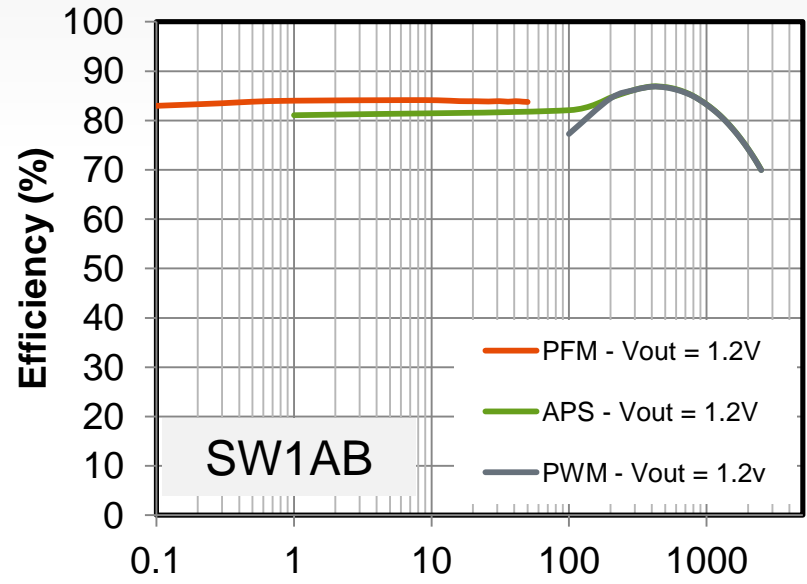
Phase Interleaving:

When the top FET in a buck converter turns on, input capacitor sees sudden discharge. By interleaving the different switching converters, **input ripple is minimized**. This interleaving is also programmable.



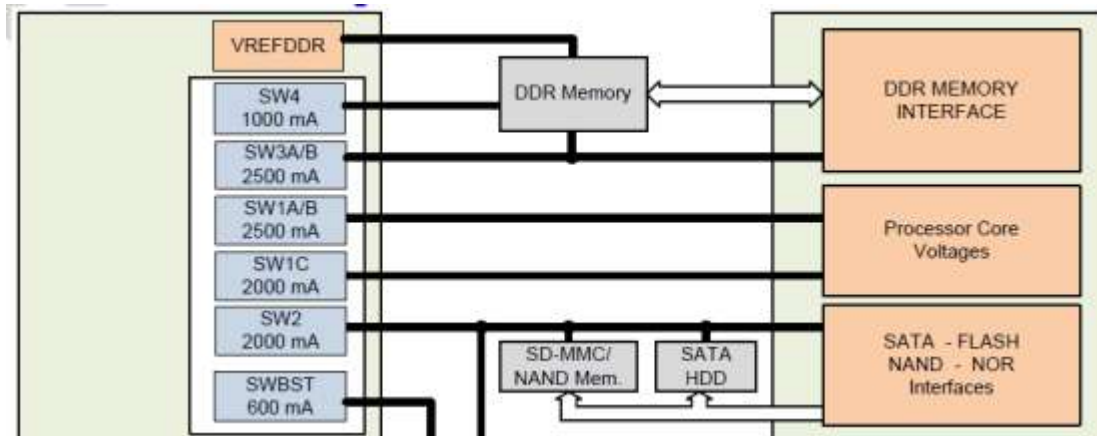


Typical Buck Regulator Efficiency



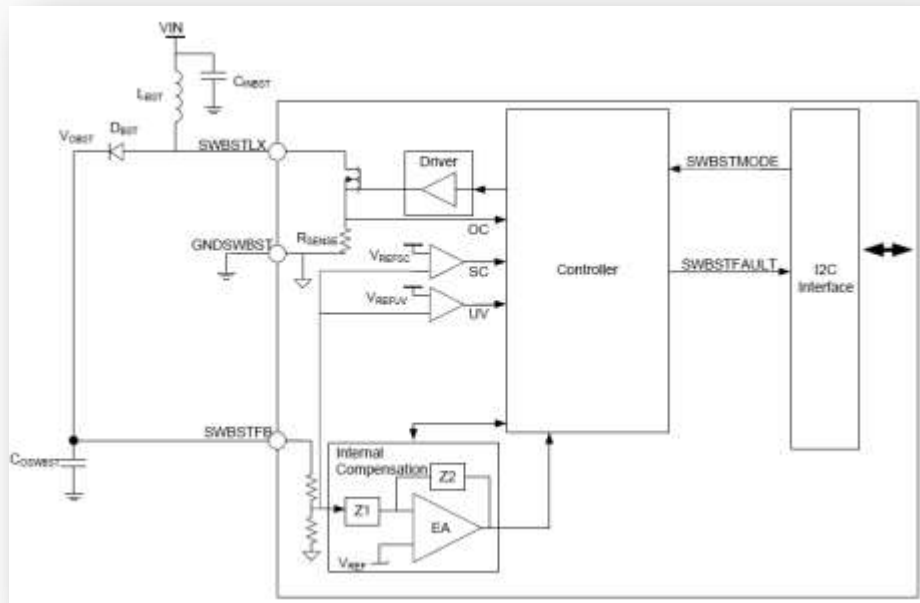
SW4 in VTT Mode

- If system requires DDR memory termination, SW4 can be used in VTT mode
- In the VTT mode, its reference voltage will track (0.5 * SW3A voltage)
- Only PWM switching is allowed in VTT mode to allow current sinking
- The VTT mode can be configured by use of VTT bit in the OTP_SW4_CONFIG register



MMPF0100 Boost Regulator

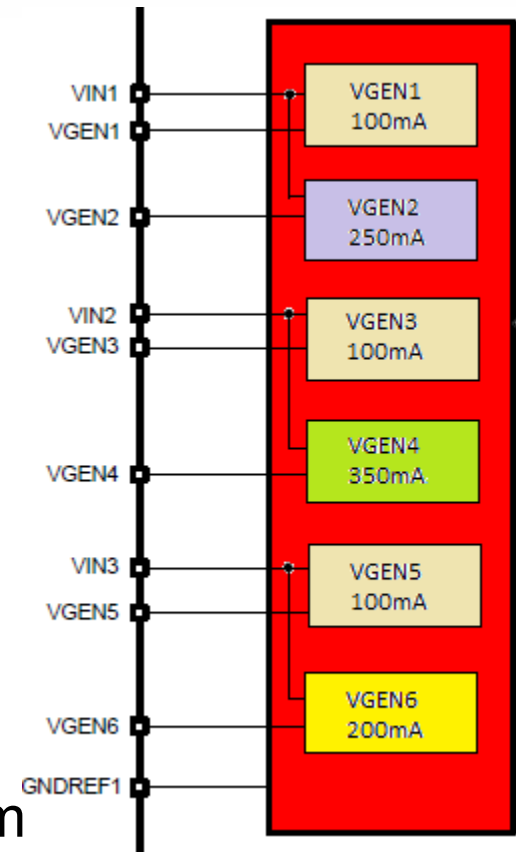
4-6 Buck switchers 2 x 1.25A 1 x 2.5A 1 x 2.0A 1 x 2.0A 1 x 1.0A Programmable Vout	1 Boost switcher 5V, 600mA	6 General Purpose Regulators 3 x 100mA 1 x 200mA 1 x 250mA 1 x 350mA
Interface On/Off Reset Stand-By Interrupt	PF0100	Memory OTP memory
Coin Cell Coin cell charger RTC supply – 400uA	Control Logic Fully programmable voltage, current, timing sequence I2C interface	Reference Generator Internal clock and analog reference



Programmable output voltage
 5.0V/5.05V/5.10V/5.15V
 600mA
2MHz Switching Frequency
 Modes: PWM, PFM, AUTO
OCP fault interrupt

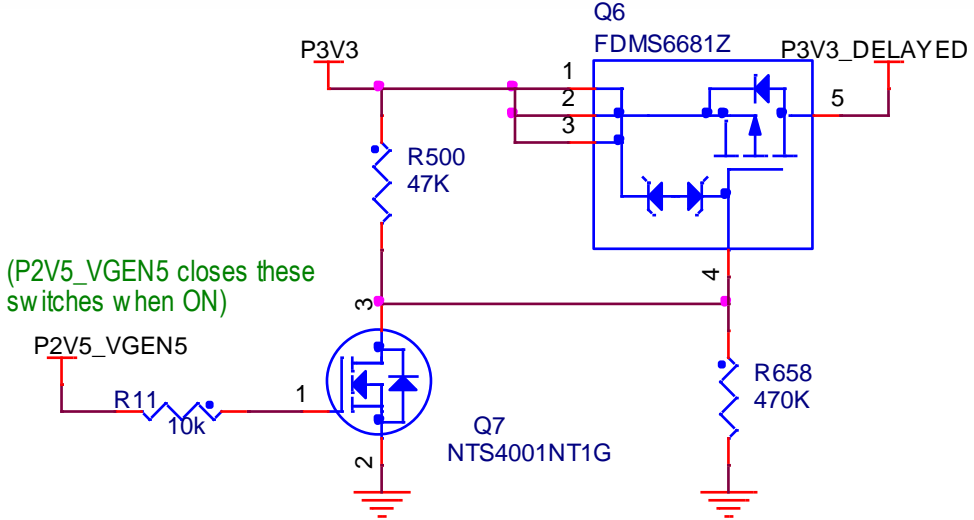
VGENx LDO Specifications

- Programmable output voltage
 - VGEN1, 0.80V - 1.55V, 100mA
 - VGEN2, 0.80V - 1.55V, 250mA
 - VGEN3, 1.8V - 3.3V, 100mA
 - VGEN4, 1.8V - 3.3V, 350mA
 - VGEN5, 1.8V - 3.3V, 100mA
 - VGEN6, 1.8V - 3.3V, 200mA
- Soft start – output slew rate control
- Low power mode, automatically or setting by the VGENxLPWR bit
- Short circuit/Over current protection
- Unused LDO's can be used for general system sequencing!



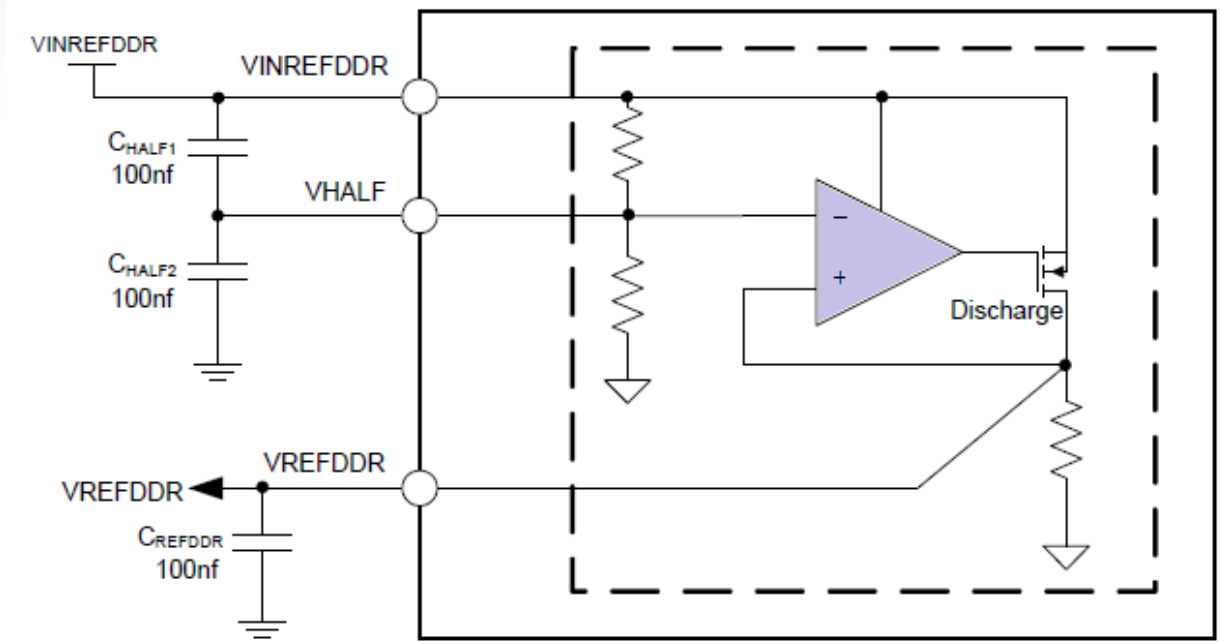
Using Unused LDOs for Sequencing

- The PF0100 has 6 general purpose low dropout linear regulators
- The startup sequence of these LDO's can be OTP programmed
- Output of these LDOs can be used to drive an external bypass FET to control the sequence of other power rails in the system



Optional Circuit for using VGEN5 as a sequencer. P3V3 and P3V3_DELAYED are shown for example. The concept can be used for other system rails.

VREFDDR Voltage Follower



- 10mA Current capability
- Output voltage tracks half of the input voltage

Parameter	symbol	Min	Typ	Max	Unit
VREFDDR					
Operating Input Voltage Range	$V_{INREFDDR}$	1.2		1.8	V
Operating Current Load Range	I_{REFDDR}	0		10	mA
Current limit $V_{INMIN} < V_{IN} < V_{INMAX}$ $V_{REFDDR} = 0.5 * (V_{INREFDDR})$	$I_{REFDDRLIM}$	11.25	15	18.75	mA

MMPF0100 State Machine Modes of Operation

- **On mode.**
 - When the PF0100 is in the On mode, all functionality is available. RESETBMCU is high.
- **Off mode.**
 - Only VCOREDIG and the coin cell module are powered. A valid turn-on event can exit the OFF mode.
- **Standby mode**
 - Pin on PMIC: STANDBY
 - Enter Standby mode: STANDBY is asserted high when the SOC enters low power mode .
 - Exit Standby mode: STANDBY is de-asserted. Supply is expected to regulate to previous voltage.
- **Sleep mode**
 - Pin on PMIC: PWRON
 - Enter sleep mode: PWRON is de-asserted low when the SOC enters sleep mode.
 - Exit sleep mode: PWRON is asserted high.
- **Coin cell mode**
 - VIN=0V and the coin cell is the only valid power source to the PF0100.
 - No turn-on event is accepted.
 - RESETBMCU is low.
 - VCOREDIG is at ~1.3V.

